Part II
Chip-to-chip Signaling On-Package
23.3 A 0.54pJ/b 20Gb/s Ground-Referenced Single-Ended Short-Haul Link in 28nm CMOS for Advanced Packaging Applications

John W. Poulton, William J. Dally, Xi Chen, John G. Eyles, Thomas H. Greer III, Stephen G. Tell, C. Thomas Gray

NVIDIA Corp.
Outline

- Motivation
- Ground-Referenced Signaling (GRS)
- GRS circuit details
- Test chip results
- Conclusion
On-Package Signaling

Backplane

Package-to-Package

Chip-to-Chip on Package
Motivation

• Addresses some fundamental problems with..
  • Processor-to-processor links
  • Processor-to-memory links
• Industry-standard I/O no longer improving
  • PCIe: 8Gb/s, 20pJ/bit or higher
  • GDDR-5: 7Gb/s, 15-20pJ/bit
  • To keep up: need >25Gb/sec @ < 1pJ/bit
• Attack the problem in packaging domain
  • Co-design package/interconnect/circuitry
Motivation

- High-speed, low-power on-package interconnect..
- ..addresses fundamental problems in graphics H/W

Cost, Flexibility

Memory B/W
Motivation..

• Break big chips into little ones?
  • Cost.
  • Defect density is no longer dropping, so big chips are increasingly expensive

• Breakout by function.
  • Time to market.
  • Different parts (GPU’s, CPU’s, I/O, Memory)…
  •.. designed and brought to market
  •.. on different schedules, different technologies
Laminated Packages

- Chip
- C4 Bumps (200µ centers)
- Laser-drilled blind vias
- PTH’s
- Thick Core
- Solder Balls (1mm centers)
- Build-up Layers
- 20µ line/space stripline
- 2-between breakout
Top-Layer Chip-to-Chip Channel

36-port EM Analysis (HFSS), complete 10mm channel

Insertion Loss: 1.6 dB
X-talk: 28 dB
What’s Needed:

Given benign channel:

A chip-to-chip signaling systems that is:

• Essentially free (area, power)
• As high speed as possible (conserve bumps)

Characteristics:

• Single-ended (SE) signaling
• 20-25 Gb/sec rate
• Terminated at both ends
• Very low swing
• Circuit-, not channel-limited
• Only minimal signal integrity features
Isn’t Single-Ended Signaling Bad?

- Reducing pin-count so compelling that it’s worth re-visiting
- What’s needed is a way to deal with SE’s fundamental problems..
- Revisit:
Problems with SE Signaling

1. Reference Problem
   - Hard to get Tx and Rx to agree
   - Noise couples asymmetrically to signal and Vref
Problems with SE Signaling

2. Return Problem
- Complex, split current return path
- Poor termination, cross-talk
Problems with SE Signaling

3. Simultaneous Switching Problem
   - Data-dependent current generates noise on supplies
   - Coupled to other signals via supplies
   - Proportional noise source!
Ground-Referenced Signaling (GRS)

Reference Problem: GND lowest Z, most robust network in a system, so Tx and Rx can easily agree on Vref.

Return Problem: Signal current stays with image on GND plane, flows only through terminators and ±Vs supplies.

Simultaneous Switching Noise (SSN) Problem? How to generate ±Vs?
GRS Transmitter

GRS transmitter combines
- Line driver
- 2:1 mux
- Charge pump
GRS Transmitter Operation

Precharge
clk = HI
**GRS Transmitter Operation**

Drive Out
clk = LO
d0 = LO
GRS Transmitter Operation

Drive Out
clk = LO
d0 = HI
Simultaneous Switching Noise

- Each capacitor charged on each clock cycle
- ..regardless of data to be transmitted
- Supply current independent of data
- So.. No SSN
- There will be ripple on the line..
- ..but @ bit-rate; doesn’t affect eye height
• Junctions get forward biased
• “Off” transistor gets turned on
• .. For typical signal levels, only 10’s of μA’s
Parasitic Capacitance Effects

Driving HI: CTOP discharge & CBOT charge, add to signal current.

Driving LO: CTOP discharge and CBOT charge, subtract from signal current.

Result: transmitter offset.
Parasitic Capacitances..

- Tx voltage offset $\sim \frac{C_{\text{para}}}{C_{\text{drive}}}$
- $\sim 10\%$ of P-P signal voltage
- Could compensate at transmitter:
  - Separate C’s for HI and LO drive
- Or compensate at receiver
  - Treat as systematic offset

![Graph showing voltage levels](image)
What Happens at Lower Speed?

Avg current $\propto V_{\text{supply}} \times C_{\text{drive}} \times F_{\text{req}}$

Address with:

- Hysteresis at receiver (problematic for noise)
- Add shunt capacitance, along with EQ
- Always operate at full speed and...
  ... throttle by turning link on/off

At low freq, signaling becomes RZ
GRS Tx Details

NMOS Depletion Caps
50fF each

4.1μ

Precharge

10μ

Capacitors

Bridge

Logic

8 Tx Segments

~1mA line current per Tx segment @ 20Gb/s

~50% efficient, supply current to line current
Charge pump itself is ~90% efficient
Adding EQ

W-element, 3” FR-4
-10dB @ 10GHz

“Linear” Tx Equalizer
Receiver

- Matched (Ideally)
- Gain ~ 5
- Common-Gate Amp
- Gain ~ 2
- CMOS Output
- Termination
- Offset trim

- Consumes ~ 0.7mW
Test Chip Summary

- TSMC 28HP (28n) CMOS
- 20Gbit/sec operation at 0.9V
- 0.54pJ/bit energy consumption
- 0.11mm$^2$ area for 16+2 I/O macro
- 30Gbytes/sec B/W per mm chip edge
- “CMOS” mode at 2Gb/sec
- No EQ, no ESD (both added easily)
- No clock recovery, no de-skew (not needed)
Test Chip Overview

- **txdat**
- **txclk**
- **rxdat**
- **rxclk**
- **clk{P,N}**
- **data**

Symbols:
- DIV: Division
- φ: Phase
- UI: Unit Interval

Note: The diagram shows a test chip overview with signals connected as follows:
- txdat and txclk are input signals.
- The signals are divided by 8.
- Data (1 of 16) is transmitted.
- rxdat and rxclk are output signals.

Additional notes:
- LC Osc: LC Oscillator
- DIV8: Division by 8
- φ: Phase
- UI: Unit Interval
- ~½ UI: Approximate half unit interval
- ½ UI: Half unit interval
- 2: Signal level

The diagram illustrates the flow of data through the chip with annotations for clarity.
## Power Breakdown

<table>
<thead>
<tr>
<th>Component</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage</td>
<td>0.45 mW</td>
</tr>
<tr>
<td>Oscillator</td>
<td>0.75 mW</td>
</tr>
<tr>
<td>Distribution</td>
<td>4.5 mW</td>
</tr>
<tr>
<td>Clk Total</td>
<td>5.7 mW *</td>
</tr>
<tr>
<td>Transmitter</td>
<td>3.2 mW *</td>
</tr>
<tr>
<td>Receiver</td>
<td>1.9 mW *</td>
</tr>
<tr>
<td>Total</td>
<td>10.8 mW</td>
</tr>
</tbody>
</table>

@ 0.9V supply, 20Gb/s operation, 150mV P-P signal, includes all SER and DES logic
BER Measurements

2 Tx segments  3 seg’s  4 seg’s  5 seg’s

BER

Phase (UI)
I/O Macro

- Terminators
- Bypass Cap
- Rx
- Bypass Cap
- Tx
- Data Transceiver
- Clock Buffers
- Connections to LC Osc
- Diff Clock Transceiver
- 57.2µ
- 514.8µ
- 114.2µ
- 228.4µ
Test Chip

- Equal-length (-cap) RDL, macro to bumps
- JTAG IO
- Standard cell logic
- High speed bumps
- 16 lane I/O macro
- 3mm
- Osc/clock macro
- Osc Inductor
- Vdd bumps
- GND bumps

Dimensions: 2mm width, 3mm height
Test Package

Scope probe points

Equal-length RDL traces from I/O macro to bumps

Test Chip

HDI signal traces within package

Blind vias

Laminated Package

PC Board

3mm

4.5 mm
GRS Factoids

• “CMOS” circuitry only
  • Uses only core transistors
  • Friendly to future technologies
  • ..where “current-mode” analog doesn’t work
• Easy to interface between
  • Different semiconductor processes..
  • ..operating at different supply voltages
• Should be effective on Si Interposers
More GRS Factoids

• Charge-pump idea works for differential, too.
• Basically a sort of floating Norton source
• Can put the common-mode voltage anywhere that’s convenient
• Perhaps an alternative to “current-mode” and “voltage-mode” signaling approaches
Summary

• Single-ended, ground-referenced signaling
• Implemented with novel charge-pump transmitter
• 20Gb/sec, low BER, low power (0.54pJ/bit)
• Small area PHY (0.11mm² per 16 bits)
• 30GBytes/sec B/W per mm of chip edge
• Some challenges (and opportunities) operating at lower rates
Probe Station

Package on Board

45 x 45 mm Laminated Package