Memory Circuits

Dr. Paul D. Franzon

Outline

• DRAM
• NV memories

References

• Kang & Leblecici, CH 10
• Itoh, VLSI Memory Design
• Micheloni, Mareli, Ravasio, Error Correction Codes for Non Volatile Memories
DRAM

Bit line equalizer

Memory Cell Array

Row Decoder

PSA

PSAB

Vdd/2

Bit line Sense Amp

SAB

SA

PISO

PEQ

WL0

WL255

CS

BL

BLB

Vp

C

Cs

Vdd/2

(precharges to Vdd/2)

Vdd/2

Sense Amp Equalizer

PSAEQ

BL_J0

BL_J0B

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PEQ/PSEQ

PSIO

WL

BL/BLB

PSA

PSAB

CS

BL_IO/B

Restores Cell Data

Amplified to Outputs
**Read Operation**

Why is PSIO “overboosted” to $V_{pp} > V_{dd}$?

What is the swing on BL at time A?

What happens at time B?

What happens at time C?

What happens at time D?
Write Operation

Same as Read

\[ BL/BLB \]

\[ CS \]

\[ BL_{IO}/BL_{IOB} \]

BL_{IO}/B overcomes latch in sense-amp
**DRAM Organization**

Hierarchical Memory:
- DRAM cells organized into blocks with locally buffered row address decoders and local sense amps
- Bank has an array of blocks with global address lines and global sense amps

Sequence of operations (read):
- Row address applied
- Row is “opened” and read into latches at bottom of banks
- Column address applied
  - Word read
- While row is “open” several words can be read out quickly as a “burst”
Flash Memory

Charge stored on floating gate changes $V_t$

Programming through hot electron injection:
- High lateral field $\Rightarrow$ Avalanche breakdown generates hole/electron pairs. Electrons injected into floating gate via high gate field

Program via tunneling:
- Apply high $V_{pp}$ to D or S
- Electrons tunnel
Flash Memory Operation

Changing charge stored on floating gate changes $V_t$:

$$\Delta V_T = \frac{\Delta Q}{C_{FG-CG}}$$

- $VR$ enough to turn “1” gate on but “0” gate off
NOR Flash RAM

Program:
- Hot electron
- \( \text{BL}=1 \, \text{V}; \, \text{WL} = 12 \, \text{V}; \, \text{SL} = 0 \, \text{V}; \)

Erase:
- Tunneling
- \( \text{BL}=\text{open}; \, \text{WL} = 0 \, \text{V}; \, \text{SL} = 12 \, \text{V}; \)

Read:
- \( \text{BL}=1 \, \text{V}; \, \text{WL}=5 \, \text{V}; \, \text{SL}=0 \, \text{V} \)
- Gives \( \text{IDS} > 0 \) if “0” stored

Not Read:
- \( \text{BL} \) and/or \( \text{WL} = 0 \text{V} \)

Need current amplifier for sense amp
NOR Sense Amp

Compare with a reference cell programmed mid-way between “1” and “0”

- SAEN’ → 0
- M1/M2 turns on
- Limits Vds of FG transistor, preventing inadvertent state change
- Output = I_DS(FG)*R
- Comparator

![NOR Sense Amp Diagram]
NAND Flash RAM

Program:
- Tunneling
- BL=0V; WL = 20 V; SL = 5 V; source Line = 0
- Other WL = 10 V

Erase:
- Tunneling
- BL=0V; WL = 0 V; SL = 5 V; source Line = open; pwell = 20 V
- Other WL = 10 V

Read
- 0V applied to selected WL; 5 V to other
- Will complete pull down path if 0 stored

Smaller; slower and less scalable than NOR flash structure
NAND Read

Current very low – NOR circuit would not work

1. Mp on – precharge Vout
2. VMn= V1
   - If cell pulling down, pulling down VBL (evaluate phase)
3. VMn=V2
   - If VBL < V2-Vt, Mn turns on pulling Vout down to VBL (read phase)

Note:
- If Icell = 0, Mn stays OFF in read phase