ECE 733
Project 2

Transceiver Design

Design a 1-bit wide 45 nm differential transceiver that meets the following constraints and goal:

- Operating over a 100 cm long lossy differential transmission line, with 0.25 pF of load capacitance added at each end (to represent pad capacitance).
- Operating at an actual data rate of at least 4.0 Gbps while meeting the template on the next page for a BER of better than $10^{-12}$.
- Your design GOAL is to minimize the metric $\text{energy} \times \text{BER}$ for the data sequence below. Your power must include all components in your design.
- You should design and build current mode logic flip-flops for this project. There are no specific requirements on setup, hold and ck-Q delay. The power of the flip-flops is included in your design.
- Use the device Spice Models from project 1
- While meeting an eye specification of an eye aperture opening, measured by the Cscope tool, specified below (as measured at the final output of your RX BEFORE data recovery) while executing the following 128-bit sequence (the gaps are to add readability):
  - 0101 1001 0100 1100 0001 0000 0101 1111 0111 1100 0101 0001 1100 0011 1101 0101 REPEATED TWICE
  - Note: The maximum run length in this sequence is 5 bits. I ask for a 128 bit sequence so as to ensure plenty of opportunities for ISI due to reflection noise.
  - You can use the “.include” feature in Hspice to read in a data file generated elsewhere.
- You have data complementary inputs operating at 4 Gbps.
- Correct transistor perimeter and area parameters must be included in the spice netlist.
- Ideal voltage and current sources cannot be used to supply biases to internal circuitry. However, ideal spice implementations can be used for bandgap reference and OpAmp designs if used.
- All clocks must be buffered by an inverter so as to give a reasonable rise time. (You can resize the transistors in this pair.) THIS INVERTER IS TO BE INCLUDED IN YOUR POWER CONSUMPTION.
- All inputs should have rise and fall times of 30 ps.
- Use the differential circuit structure, with resistor compensation, as defined in the class notes.
- Temperature $= 90$ C

Otherwise, you are free to use any technique you see fit, including differential circuits, equalization, termination, coding, etc. (Note if you use coding, you must report the effective data rate, and achieve at least 4 Gbps in that rate, not the coded rate).
**Required Eye Opening at final RX output**

You must achieve the following eye opening at the RX output, before any resynchronization flip-flop. This is a differential eye.

![Eye Diagram](image)

The eye diagram versus Bit Error Rate (BER) tradeoff is summarized in the following table:

<table>
<thead>
<tr>
<th>∆V</th>
<th>∆T</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>400 mV</td>
<td>0.9 UI</td>
<td>2*10^{-13}</td>
</tr>
<tr>
<td>300 mV</td>
<td>0.85 UI</td>
<td>5*10^{-13}</td>
</tr>
<tr>
<td>200 mV</td>
<td>0.8 UI</td>
<td>10^{-12}</td>
</tr>
</tbody>
</table>

This is measured at the RX input.

**Deliverables**

A report describing the approach used, including circuit topology, design procedure, simulation results, and achieved speed. All results should be presented in the
body of the report (in tables if possible). Relevant schematics, plots, netlists, text files, etc. should be clearly referenced and included in the appendix. Binary text files do not need to be included.

- It is important to document your design procedure.
- Please include an eye diagram, showing the points that lie outside of the template above for your claimed $\Delta V$ and $\Delta T$.

**Evaluation**

You will be evaluated out of 100 and assigned a grade based on the following criteria:

80: This is the grade that will be given to a basic, working complete project. I.e. If it meets the constraints described above.

70-79: Missing one or two major attributes above. E.g. Being slower.

0-69: A submission that clearly does not achieve the goals established here. E.g. Does not work, very slow maximum speed.

10 additional points are allocated for the quality of the report. This brings the base grade up to 90.

Up to 15 bonus points are earned competitively based on power consumption, EXCEPT FOR THE FLIP-FLOPS. The worst power will earn 0 points, the best 15, and those in between will get bonus points on a linear scale. Note, you can earn 105 points for this project.

**Collaboration**

If you help each other that is fine, in fact encouraged. However, I expect that each of you do your own design, design capture, optimization, simulations and interpretation for the final report. I further expect each design to be unique, at least on the details of transistor sizes. If it is clear that someone rode completely on another students work, both students will be penalized. I request that you DO NOT share electronic versions of your designs or results. E.g. Explaining, in detail, how your design works to a friend is good, emailing that friend your schematic file is very bad and, if discovered, will be considered an academic violation.

**Recommended Design Procedure**

*Step 1. Termination and equalization design.*
The main tool in reducing ISI is analyzing the pulse response of the circuit. Take the Tline model given in the accompanying Spice file, add in the 0.25 pF of capacitance at each end, and design a suitable single stage differential amplifier TX and RX. Apply a 010 pulse at the driver and observe the time domain response at the RX. Observe the pulse response for at least 128 bit periods, so you have a chance of seeing reflection noise. You should see a pulse response something like this (note I have normalized the 010 swing at the RX for the bit pulse to be 1):

![Pulse Response Diagram](image)

The bumps that are many bits out are due to reflection and the tail-end of the initial pulse response is due to the channel response. You should eliminate those first by using appropriate terminations. Options include terminating at one end only or both ends, terminating just the differential mode or both the DM and CMs. Note, I gave no common mode requirements on the input eye; the RX has good common mode rejection.

Resimulate after you have decided on the appropriate termination. You have now have to design equalizer. You can take a first stab at the equalizer by looking at the ISI following 1 UI (UI’s 2, 3, and 4 here). The role of the equalizer is simply to reduce this ISI to acceptable levels. The easiest way to do this is simply to subtract out the expected ISI by using the following filter:

\[ 1 - a_1 z^{-1} - a_2 z^{-2} - a_3 z^{-3} \]

Etc. Note here I use a 3-tap filter. You might desire more or fewer taps depending on the ISI that you see.

You should then implement this filter in Spice, using perfect sources and check the pulse response has minimal ISI.

Alternatively, you can design the filter in the frequency domain if you wish. The objective is a flat band pass and linear phase response over the frequency content of the data.

**Step 2. Circuit Design**

Now implement a driver circuit that satisfies this bandwidth, swing and eye opening specified above. In your report describe the initial design of the circuit and how you traded off swing, bandwidth, and power. Describe how you biased and sized the current
mirrors and reference circuit, and any other circuits you use. Clearly show how the Spice simulation that resulted from your initial design was used to guide the steps towards the final design.

**Background References**


Text portion is limited to FOUR ages, 12 point font, 1” margins. Use additional pages for figures as needed.

Title, Name

Abstract. Summarize key results. E.g. “This report describes ...”

1. Introduction
Introduce purpose of project, and outline of report. Your target audience is a potential employer, not a project evaluator.

2. Technical Approach
Describe how you approached the design and iterated on it until you obtained the desired results.

3. Key Simulation results
Show annotated simulation results clearly supporting claimed timing and power numbers.

4. Conclusions
Brief conclusions describing what was achieved and any unique features demonstrated.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Horizontal Eye</th>
<th>Vertical Eye</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX/RX</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 1. Eye Diagram. Mark required template clearly on waveforms.

Figure 2. Pulse response before equalization, showing tap weight calculation.

Figure 3. Final Schematic (full page). Transistor sizes clearly readable.

Figure 4. Pulse response after equalization.

Other figures can be included as needed.

Appendices
Spice Netlist (pages as needed)

Result File (.mt0)

Plot of power consumption