ECE 733: Digital Electronics  
Spring 2004  
Course Overview & Policies

Class Schedule: Tuesday, Thursday, 4.30 – 5.45 pm, DAN 406

Instructor: Professor Paul D. Franzon, Ph.D.  
Office: EGRC 443, (919) 515-7351  
E-mail: paulf@ncsu.edu  
Home page: www.ece.ncsu.edu/erl/faculty/paulf.html  
Office Hours: Tuesday, Thursday 6.00 – 7.00 (in DAN 348); after 8.30 (DAN 429)

Lab TA/Graders: To be announced. Due to the size of this class, please use the wolfware bulletin board and the TAs as your first point of contact to resolve lab and HW questions.

Textbooks & Notes:  
References include the following:  

Course notes, papers, project assignments, etc.: The wolfware course locker will be used to distribute course notes, papers, and assignments. Please make sure that you print the first set of notes before the first class from the website. Also note that the notes distributed on-line are NOT the complete notes for the class. Classroom attendance and note-taking is expected.

Prerequisite: Grade of C or better in ECE 302 or equivalent. Functionally, I am assuming that students are familiar with the basics of MOSFET operation and MOSFET circuit design, e.g. linear and saturation modes, and the design and operation of CMOS static logic gates. I will assume that you also have access to, and know how to use, a suitable circuit simulator, such as Hspice. Knowledge of how to use a schematic capture tool would be highly useful too.

Course Objectives. Provide an in depth study of selected topics in the design of digital circuits, at the transistor level. The topic list is not finalized at this point, but is likely to include digital circuit fundamentals; SOI families; high-speed flip-flops and Serial-Deserializers; RAM; I/O transceivers; clock distribution; and clock and data recovery, including PLL design. If time permits there will be some review of future nanoelectronics digital circuits.

Course Approach: This is a Ph.D. level course. As such, it will mainly emphasize learning through studying digital circuits through published papers. After some initial, more lecture-style material, much of the classes will focus on an instructor lead discussion of selected papers. You will be expected to review the selected papers before each class. You will find this class less structured and faster paced than my lower-level offerings. It will focus a lot on developing the skills to learn from relatively unstructured material (a/k/a research papers). This is intentional.

In order to provide an in-depth experience, you will also carry out two small design projects. The projects are not finalized yet but are likely to be a high-speed CMOS flip-flop design, and a CMOS transceiver design. An informal lab will be organized to provide active help for the projects and provide a forum for evaluation of the projects. Though lab attendance is not required, little assistance will be available outside of the labs.
**Student Evaluation.** You will be evaluated as follows:

- **Homeworks.** There will be a small number of homeworks to force review of specific issues. (20%)
- **Midterm.** (20%)
- **Projects.** You will be individually graded on two small projects. Each project is worth 20% of the grade. (40%).
- **Final exam.** On material covered since the midterm. (20%)

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<thead>
<tr>
<th>Exam Type</th>
<th>Date</th>
<th>Time</th>
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<tbody>
<tr>
<td>Midterm Exam</td>
<td>March 6</td>
<td>In class</td>
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<tr>
<td>Final Exam</td>
<td>Thursday, May 6</td>
<td>1-4 pm</td>
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Collaboration are encouraged on the homeworks and projects but you are expected to turn in individual solutions and reports. The exams will be open-book, open-notes, multiple-choice exams.

**Important Dates**
- No class on April 8
- Spring Break: March 8-12.
- Last day to drop: March 19
- Last class: April 29

**Instructor Research Interests**
- Interconnect, including transceivers, electronic packaging, on-chip interconnect, optical & electronic interconnect, network switch ICs, MEMS-based interconnect.
- Circuit design, including low-power, SOI, moletronic circuits
- Sample projects:
  - AC Coupled Interconnect
  - On-chip interconnect design
  - Ultra-low power, low-noise SOI radio baseband circuits and architectures
  - Switch architectures for next generation optical networks
  - Molecular circuit design and construction

**Students with disabilities**
Reasonable accommodations will be made for students with verifiable disabilities. In order to take advantage of available accommodations, students must register with Disability Services for Students at 1900 Student Health Center, Campus Box 7509, 515-7653. [http://www.ncsu.edu/provost/offices/affirm_action/dss/](http://www.ncsu.edu/provost/offices/affirm_action/dss/) For more information on NC State's policy on working with students with disabilities, please see [http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html](http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html)

**Academic integrity**
All the provisions of the [code of academic integrity](http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html) apply to this course. In addition, it is my understanding and expectation that your signature on any test or assignment means that you neither gave nor received unauthorized aid.