Design Alternatives

Timing Scenarios (Clocking strategy)
- Master synchronized clock
- Source synchronous clocking
- Clock Recovery

Basis for Signaling Circuit
- Voltage Mode vs. Current Mode
- Single sided vs. Single sided against reference vs. Differential

Termination
- Source vs. Load vs. On-chip

Direction
- Single direction vs. Bidirectional

Data Representation
- Non Return to Zero vs. Return to Zero vs. Pulse vs. N of M Code (e.g. 8b/10b)
- Pulse Amplitude Modulation: PAM-2 (binary) vs. PAM-4 (4-level)

Use of Channel Compensation
Use of Error Correcting Codes
Case Study – AC-Coupled Interconnect (ACI)

Timing Scenarios
- Sufficient delay slack for noise to settle:

- If $t_{\text{interconnect-max}} < 5 \times \text{line delay}$, then design is very simple.
- First Incident Switching:

- $V_{\text{hi}}$
- $V_{\text{lo}}$
- 50% Delay
- V-50%
Source-Synchronous Switching

- Send clock with data
  - (or recover clock from data)

- In such systems, the rise-times and skew from inter-symbol noise, processing and temperature variations determines maximum signal speeds

E.g. 1 Gbps, 30 inch wire

\[ t_{\text{symbol}} = t_{\text{wire}} = \]

If clock jitter has to be less than 10% of \( t_{\text{symbol}} \), \( t_{\text{jitter}} = \)

What % variation in clock “\( t_{\text{wire}} \)” would be acceptable?

If a via \( C_L = 1 \) pF, \( Z0 = 50 \) Ohm, what is the \( \tau \) of a via?

Clock & Data Recovery

- Recover clock from the data so that delay does not need to be precisely controlled.

- Issues:
  - Ensuring enough edges in data signal to generate clock
  - Design of clock recovery circuit (Phase Locked Loop, Delay Locked Loop)
Voltage vs. Current Signalling

- RX sensitivity 300 mV
  - Vout = A Vin enough to provide full swing at O/P
- Energy per transition, Esw = ∆V^2t_line/Z_0 = ∆I^2t_lineZ_0

Comparison: (Ignore lines losses)
- Voltage Mode, Series Termination
  
- Voltage Mode, Parallel Termination

Voltage vs. Current Mode

(i.e. Portion of constant current source fed onto line)
- Current Mode, series termination
  - Requires current-mode RX (i.e. Low input impedance)
- Current mode, parallel termination
  - Line swing and power:
    \[ V_{sw} = Z_0 I_{out} \]
    \[ E_{sw} = I_{sw^2} t_{line} Z_0 \]
- RX swing
  \[ V_{sw} = R_{term} I_{out} \]

Sample Comparison (1 ns line)
- Voltage mode, 3.3 V, series term
- Current mode, 10 mA, parallel term

Esw:
**ECE 733 Class Notes**

### Single sided vs. Differential

**Cost:**
- Full differential doubles board real-estate, and pin-count

**Performance**

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<td><img src="image1.png" alt="Diagram" /></td>
<td><img src="image2.png" alt="Diagram" /></td>
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**Sensitivity:** Smallest RX input to give full swing at output (limited by gain A)

**Noise:**
- TX: Amplifies noise at input as normal
- RX: Noise on Tran line behaves as differential noise
  - Rejects CM noise on input signal

**Termination**

### Parallel vs. Series
- See above

### Off-chip vs. On-chip
- High-speed requires on-chip

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<tr>
<td><img src="image3.png" alt="Diagram" /></td>
<td><img src="image4.png" alt="Diagram" /></td>
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</table>

- How?
  - See earlier slides on resistive load
  - Common approach: Use trimming resistors and measure against an off-chip comparison

No additional reflection noise due to package delay
BiDirectional Signalling

Halves number of wires and pins!

Current Mode:

- Estimates \( V_{\text{transmit}} \) from TX and subtracts it from signal at pin
- Speed limited compared with single sided as estimate is imperfect (due to package, \( R_{\text{term}} \) mismatch, etc.) and ISI tends to be larger
- Voltage mode and differential versions

\[ TX \quad Z_0 \quad RX \]

\[ R_t \quad V_T \quad Rt/2 \]

Signal Coding

- Run length constrained and DC balanced codes
- Error Correction Coding
  - Not used much today but likely in future
  - Pulse Amplitude Modulation (PAM), NRZ vs. RZ

Reasons to constrain max # and ratio of 1’s or 0’s

- AC Coupled Signals
  - Provide sufficient edges for clock recovery
    - Max # of 1’s or 0’s in sequence known
  - Reduce SSN, return current and \( \frac{d}{dt} \)(return current)
  - Balance 01 and 10 simultaneous transitions in a bus

\[ \text{Want: Fixed } V_{\text{bias}} \]
\[ \Rightarrow \text{Average value of input signal must be known} \]
\[ \Rightarrow \text{Known ratio of 0’s to 1’s} \]
\[ \Rightarrow \text{AC balanced signals} \]
Concepts in Balanced Codes

Run Length
- Max # of 1's in sequence = r_{\text{max}}
- Min # of 1's in sequence = r_{\text{min}}
- Code referred to as (r_{\text{min}}-1, r_{\text{max}}-1) code

Bit Stuffing
- Simplest way to achieve a (0,m) code is to insert a false bit when r_{\text{max}} hit
- Requires synchronization at frame level and counters at RX and TX
- E.g. Achieving (0,2)
  - Data: 0100011110
  - Encoded data: 01000101111010
- Though reduces low frequency content, does not eliminate a DC bias drift
- Can not predict actual symbol rate
  - Can predict worst case symbol rate
    - What is it for (0,2)?

Disparity
- = # of 1's - # of 0's

Digital-Sum Variation (DSV)
- = Max. variation in disparity
- Constant DSV \rightarrow DC-balanced signal, r_{\text{max}} = \text{DSV}
- Determines low frequency components of signal
Block Codes

Nonoverlapping Block Codes
- Each block of \( n \) bits is coded as \( m \) bits with equal numbers of 1s and 0s
- Number of zero-disparity code words in \( m \) bits is \( \binom{m}{n/2} \)
- Number of input signals is \( 2^n \)
- Thus code exists if \( \binom{m}{n/2} > 2^n \)
- Code efficiency = \( n/m \)
- E.g. \( n=2, m=4 \)
  - Efficiency = 50%
- E.g. \( n = 8, m=12 \), efficiency = 67%

Running Disparity Codes
- Permits non-zero disparity in “code word”
- Constrains worst case disparity
- Disparity = disparity of current block
- Accum = accumulated disparity, including comp bit
- Compare = 1 if Disparity and Accum have same signs
  \( \sim \) (sign(accum)) if disparity = 0
- Max run length = \( 2(n+1) \); Disparity ranges over \([-3n/2, 3n/2]\)
- DSV = \( 3n \)
- 8-bit burst error occurs whenever comp bit wrong
**Spatial N of M Signalling**

Used to reduce Common Mode noise in power/ground/return system
- Reduces SSN at TX
- Reduces signal return current
- e.g. Hamming Codes

**Single Symbol Encoding**

NRZ = Non Return to Zero
RZ = Return to Zero
Ternary ➞ 3 level signaling
PAM-4 ➞ Encode bit pair (symbol) as one of 4 levels

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<td>PAM-4</td>
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</table>
Symbol Encoding Tradeoffs

- NRZ (also called PAM-2)
  - Most common
- RZ
  - Requires 2\* channel bandwidth of NRZ
  - (Only used in optical signals where BW is almost infinite)
- Ternary NRZ
  - Use against Vref in single-sided TX, differential RX
- Ternary RZ
  - DC balanced
  - Use against Vref in single-sided TX, differential RX
- PAM-4
  - Requires half channel BW of PAM-2
  - Reduced signal swing per symbol
  - Requires ADC at RX
  - Not useful unless channel BW very limited

Case Study

AC Coupled Interconnect
- NCSU Research Project
- Coding issues
- Eye evaluation
- Outline
  - Overview
  - Benefits
  - System view
  - Circuits
  - Eye Diagram analysis
AC Coupled Interconnect Concept

New Ideas

• AC coupled connections down to 70 µm pitch
• Short- or long-range capacitive or inductive coupling
• Buried solder bumps to bring chips into proximity
• High-speed, low-power current switching techniques

Basic Circuit Models

Capacitive Coupling

Inductive Coupling
Benefits of ACI

Dense I/O
- e.g. 800 power/ground, 6,000 signal per sq.cm.
- Achieve end of the ITRS today!
- Can be applied to dense connectors too

Low power
- 20% Transmit power of conventional interconnect

High Speed
- Will extend high speed SerDes

Robust
- Can achieve low Bit Error Rates

Manufacturable
- Conformable
- No change to base fabrication process and materials

System View of Conventional I/O

Typical: ~3 Gbps, 100 mW/channel link

Lossy Channel:

DSP to sharpen edge response:

Figure 3 – Typical S21, transmission plot for serial link, picture of what is happening in the frequency domain.
Conventional I/O

1 V in, 50-100 mV needed at RX

- Losses < 23 dB required

Low-pass filter

- Makes 10 Gbps, 20 Gbps etc. increasingly difficult

Energy per bit

- \( E = \frac{\Delta V^2}{Z_0} + \) overhead for circuits & DSP
- Increased by differential, analog DSP at RX

Pin-in-hole connectors

- Creates dense via field
  - Disrupts return current
  - Increases high frequency losses

ACI

ACI acts as a differentiator:

- Pulse signaling
- Energy per bit reduced
- Integrate at Receiver

ACI acts as a high-pass filter

- Compensate for line losses
- Extends useful frequency range
- Potentially avoids DSP

ACI transformers can be asymmetric

- Can accept higher line losses

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Why 80% less power dissipation?

Suppose Vpp=0.4v, R=50ohm, 6Gbps

For CCI: Power of each pulse is less than \((0.5 \times (0.2)^2)/50\)=0.4mw, totally 5 pulses in period of 10 pulse window, so average power is 0.2mW

For Traditional: Power of each ‘1’ bit is \((0.4)^2/50\)=3.2mW, totally 5 ’1’bit in period of 10 bit window, so average power is 1.6W

\(0.2/1.6=0.125\), that is 87.5% less power

For lower frequency switching, even more power saving

CCI Channel Response

CCI channel response for 10cm, 50ohm TL
Dielectric Loss become more important for High Frequency
Kühn's Receiver

Diode Feedback to Set up Local DC level and inhibit unwanted switching due to high frequency noise

Using Latch to recover data
How Kühn’s RX Works?

B: Filter out High Freq Noise
C: Recover Data by Latch
D: Buffer

INPUT

Delay 920ps

INPUT

How Kühn’s RX Works?

EYE Diagram Analysis

4b/5b Coding

5b/6b Coding

4b/5b Coding

5b/6b Coding
Codes Evaluated

### 4B5B coding

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<th>Output word</th>
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### 5B6B coding

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<td>110101</td>
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<tr>
<td>11111</td>
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Block versions.
Above, actually used a “running” version.

EYE Diagram Analysis

Highest data rate is determined by Jitter and Rising/Falling edge.
Jitter: Caused by ISI, from both coupling cap and Kuhn’s Rx.
Rising & Falling Edge: Determined by Vdd, Device (R & C).
BER: Determined by EYE Opening, jitter of sample clock.
Estimate BER by EYE

BER is expressed here by the shadow area:

Blue shadow for BER of ‘1’
Red shadow for BER of ‘0’

BER = Integration of the shadow area

Note: Here we assume the signal is gauss distributed.

\[
BER = \int_{-\infty}^{\infty} \frac{1}{\sqrt{2\pi} \sigma_1} \cdot \exp\left(-\frac{x^2}{2\sigma_1^2}\right) \, dx + \int_{-\infty}^{0} \frac{1}{\sqrt{2\pi} \sigma_2} \cdot \exp\left(-\frac{x^2}{2\sigma_2^2}\right) \, dx
\]

\[
= \frac{1}{2} \text{erfc}\left(\frac{NML}{\sqrt{2}\sigma_2}\right) + \frac{1}{2} \text{erfc}\left(\frac{NML}{\sqrt{2}\sigma_0}\right)
\]

if \( \sigma_0 = \sigma_1 = \sigma, \) \( NML = NMH = 0.6V. \)

BER = \( \text{erfc}\left(\frac{NM}{\sqrt{2}\sigma}\right) \leq 10^{-12} \quad \Leftrightarrow \quad \sigma = \frac{NM}{7} \leq 0.085V \)

BER = \( \text{erfc}\left(\frac{NM}{\sqrt{2}\sigma}\right) \leq 10^{-17} \quad \Leftrightarrow \quad \sigma = \frac{NM}{8.6} \leq 0.07V \)

How to find \( \sigma \)?

Note: Here we assume the signal is gauss distributed.

\[
\text{Area} = \frac{1}{2} \text{erfc}\left(\frac{1}{\sqrt{2}}\right) = 0.1875
\]
Summary

What are the main factor(s) that cause eye closure?

How is equalization useful?

How are current mode and voltage mode signalling different?

What are the advantages of single-sided TX, differential RX over single-sided RX?

Inter Symbol Interference (ISI) due to limited edge rate and noise.

Increases Edge Rate by inserting a HPF, reducing ISI and BER

Driving line with $\Delta I$ vs. $\Delta V$

Increased sensitivity of RX

Rejects CM noise on Gnd and Power supply at RX

... Summary

What is the advantage of a full differential system?

What are the uses of DC-balanced and run-length codes?

What is the potential advantage of PAM-4 over PAM-2?