Design Alternatives

Timing Scenarios (Clocking strategy)
- Master synchronized clock
- Source synchronous clocking
- Clock Recovery

Basis for Signaling Circuit
- Voltage Mode vs. Current Mode
- Single sided vs. Single sided against reference vs. Differential

Termination
- Source vs. Load vs. On-chip

Direction
- Single direction vs. Bidirectional

Data Representation
- Non Return to Zero vs. Return to Zero vs. Pulse vs. N of M Code (e.g. 8b/10b)
- Pulse Amplitude Modulation: PAM-2 (binary) vs. PAM-4 (4-level)

Use of Channel Compensation
Use of Error Correcting Codes

Case Study – AC-Coupled Interconenet (ACI)
Timing Scenarios

• Sufficient delay slack for noise to settle:

\[ t_{\text{interconnect-max}} < 5 \times \text{line delay} \]

• First Incident Switching:

\[ V_{IH} \]

\[ V_{-50\%} \]
...Timing Scenarios

Source-Synchronous Switching

- Send clock with data
  - (or recover clock from data)

\[ \text{data} \rightarrow D \]

\[ \text{clock} \]

- In such systems, the rise-times and skew from inter-symbol noise, processing and temperature variations determines maximum signal speeds

E.g. 1 Gbps, 30 inch wire

\[ t_{\text{symbol}} = \] \\
\[ t_{\text{wire}} = \]

If clock jitter has to be less than 10% of \( t_{\text{symbol}} \), \( t_{\text{jitter}} = \)

What % variation in clock “\( t_{\text{wire}} \)” would be acceptable?

If a via \( C_L = 1 \text{ pF} \), \( Z_0 = 50 \text{ Ohm} \), what is the \( \tau \) of a via?
Clock & Data Recovery

- Recover clock from the data so that delay does not need to be precisely controlled.

**Issues:**
- Ensuring enough edges in data signal to generate clock
- Design of clock recovery circuit (Phase Locked Loop, Delay Locked Loop)
Voltage vs. Current Signalling

- RX sensitivity 300 mV
  - $V_{out} = A \times V_{in}$ enough to provide full swing at O/P
- Energy per transition, $E_{sw} = \Delta V^2 t_{line}/Z_0 = \Delta P t_{line} Z_0$

Comparison: (Ignore lines losses)

Voltage Mode, Series Termination

Voltage Mode, Parallel Termination
**Voltage vs. Current Mode**

(i.e. Portion of constant current source fed onto line)

**Current Mode, series termination**

- Requires current-mode RX (i.e. Low input impedance)

**Current mode, parallel termination**

- Line swing and power:

  \[ V_{sw} = Z_0 I_{out} \quad E_{sw} = \frac{I_{sw}^2 t_{line}}{Z_0} \]

- RX swing

  \[ V_{sw} = R_{term} I_{out} \]

  *In a 50 Ohm system, 300 mV requires I_{out} = 6 mA*

**Sample Comparison (1 ns line)**

<table>
<thead>
<tr>
<th>Voltage mode, 3.3 V, series term</th>
<th>Current mode, 10 mA, parallel term</th>
</tr>
</thead>
<tbody>
<tr>
<td>E_{sw}:</td>
<td></td>
</tr>
</tbody>
</table>

\[ E_{sw} = 1.652 \times \frac{2 \times 1E-9}{50} = 109 \text{ pJ} \]
\[ E_{sw} = 1E-2 \times \frac{2 \times 1E-9 \times 50}{2} = 5 \text{ pJ} \]
**Single sided vs. Differential**

**Cost:**
- Full differential doubles board real-estate, and pin-count

**Performance**

<table>
<thead>
<tr>
<th>TX</th>
<th>RX</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="TX Diagram" /></td>
<td><img src="image2" alt="RX Diagram" /></td>
</tr>
</tbody>
</table>

- **TX:** Transmits substantial portion of power/gnd noise as CM noise
- **RX:** Has low CM gain ⇒ Most power/gnd noise rejected

- **Amplifies noise at input as normal**
- **Noise on Tran line behaves as differential noise**
- **Rejects CM noise on input signal**

- **V_{ref}**

- **Sensitivity:** Smallest RX input to give full swing at output (limited by gain A)
**Termination**

Parallel vs. Series
- See above

Off-chip vs. On-chip
- High-speed requires on-chip

- How?
  - See earlier slides on resistive load
  - Common approach: Use trimming resistors and measure against an off-chip comparison

---

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BiDirectional Signalling

Halves number of wires and pins!

Current Mode:

- Estimates Vtransmit from TX and substracts it from signal at pin
- Speed limited compared with single sided as estimate is imperfect (due to package, Rterm mismatch, etc.) and ISI tends to be larger
- Voltage mode and differential versions

![Diagram of BiDirectional Signalling](Reference [return] for T line)
**Signal Coding**

- Run length constrained and DC balanced codes
- Error Correction Coding
  - Not used much today but likely in future
- Pulse Amplitude Modulation (PAM), NRZ vs. RZ

**Reasons to constrain max # and ratio of 1’s or 0’s**

- AC Coupled Signals
  - Provide sufficient edges for clock recovery
    - Max # of 1’s or 0’s in sequence known
  - Reduce SSN, return current and d/dt(return current)
    - Balance 01 and 10 simultaneous transitions in a bus

Want: Fixed $V_{bias}$

- Average value of input signal must be known
- Known ratio of 0’s to 1’s
- AC balanced signals

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**Concepts in Balanced Codes**

**Run Length**
- Max # of 1’s in sequence = $r_{\text{max}}$
- Min # of 1’s in sequence = $r_{\text{min}}$
- Code referred to as ($r_{\text{min}}-1$, $r_{\text{max}}-1$) code

**Bit Stuffing**
- Simplest way to achieve a (0,m) code is to insert a false bit when $r_{\text{max}}$ hit
- Requires synchronization at frame level and counters at RX and TX
- E.g. Achieving (0,2)
  - Data : 0100011110
  - Encoded data: 01000101111010
- Though reduces low frequency content, does not eliminate a DC bias drift
- Can not predict actual symbol rate
  - Can predict worst case symbol rate
    → What is it for (0,2)?
... Concepts

Disparity

- $z = \# \text{ of 1’s} - \# \text{ of 0’s}$

Digital-Sum Variation (DSV)

- $z = \text{Max. variation in disparity}$
- Constant DSV $\Rightarrow$ DC-balanced signal, $r_{\text{max}} = \text{DSV}$
- Determines low frequency components of signal
Block Codes

Nonoverlapping Block Codes

- Each block of n bits is coded as m bits with equal numbers of 1s and 0s
- Number of zero-disparity code words in m bits is \( \binom{m}{n/2} \)
- Number of input signals is \( 2^n \)
- Thus code exists if \( \binom{m}{n/2} > 2^n \)
- Code efficiency = \( n/m \)
- E.g. \( n=2, m=4 \)

<table>
<thead>
<tr>
<th>input</th>
<th>code</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>0101</td>
</tr>
<tr>
<td>01</td>
<td>1010</td>
</tr>
<tr>
<td>11</td>
<td>1100</td>
</tr>
<tr>
<td>10</td>
<td>0011</td>
</tr>
</tbody>
</table>

Efficiency = 50%

- E.g. \( n = 8, m=12 \), efficiency = 67%
Running Disparity Codes

- Permits non-zero disparity in “code word”
- Constrains worst case disparity

- Disparity = disparity of current block
- Accum = accumulated disparity, including comp bit
- Compare = 1 if Disparity and Accum have same signs
  = ~(sign(accum)) if disparity = 0
- Max run length = 2(n+1); Disparity ranges over [-3n/2, 3n/2]
- DSV = 3n
- 8-bit burst error occurs whenever comp bit wrong
Spatial N of M Signalling

Used to reduce Common Mode noise in power/ground/return system

- Reduces SSN at TX
- Reduces signal return current
- e.g. Hamming Codes
Single Symbol Encoding

NRZ = Non Return to Zero
RZ = Return to Zero
Ternary ➔ 3 level signaling
PAM-4 ➔ Encode bit pair (symbol) as one of 4 levels

<table>
<thead>
<tr>
<th></th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>NRZ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RZ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ternary NRZ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ternary RZ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PAM-4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Symbol Encoding Tradeoffs

- NRZ (also called PAM-2)
  - Most common
- RZ
  - Requires 2* channel bandwidth of NRZ
  - (Only used in optical signals where BW is almost infinite)
- Ternary NRZ
  - Use against Vref in single-sided TX, differential RX
- Ternary RZ
  - DC balanced
  - Use against Vref in single-sided TX, differential RX
- PAM-4
  - Requires half channel BW of PAM-2
  - Reduced signal swing per symbol
  - Requires ADC at RX
  - Not useful unless channel BW very limited
Case Study

AC Coupled Interconnect

- NCSU Research Project
- Coding issues
- Eye evaluation
- Outline
  - Overview
  - Benefits
  - System view
  - Circuits
  - Eye Diagram analysis
New Ideas

• AC coupled connections down to 70 µm pitch
• Short- or long-range capacitive or inductive coupling
• Buried solder bumps to bring chips into proximity
• High-speed, low-power current switching techniques

1. Want to AC couple signals but maintain DC connections
2. Need AC pads close to substrate
3. Buried solder bumps enable both
4. Inductive or Capacitive coupling
Driver is simple cascaded inverter stage
Center pad chip1 to center pad chip2 -> C_{couple} = 21 fF
pad to pad parasitic -> C_{parasitic} = 2.4 fF
pad to chip ground -> C_{shunt} = 2.5 fF
This assumes no metal underneath the pads
Chip to Chip spacing is zero, but pad to pad spacing is 3.4um
- this is due to the thickness of each chip’s passivation layers
Benefits of ACI

Dense I/O
- e.g. 800 power/ground, 6,000 signal per sq.cm.
- Achieve end of the ITRS today!
- Can be applied to dense connectors too

Low power
- 20% Transmit power of conventional interconnect

High Speed
- Will extend high speed SerDes

Robust
- Can achieve low Bit Error Rates

Manufacturable
- Conformable
- No change to base fabrication process and materials
System View of Conventional I/O

Typical: ~3 Gbps, 100 mW/channel link

Lossy Channel:

DSP to sharpen edge response:

Figure 3 – Typical S21, transmission plot for serial link and picture of what is happening in the frequency domain.
Conventional I/O

1 V in, 50-100 mV needed at RX
- Losses < 23 dB required

Low-pass filter
- Makes 10 Gbps, 20 Gbps etc. increasingly difficult

Energy per bit
- $E = \Delta V^2/2Z_0 + \text{overhead for circuits & DSP}$
- Increased by differential, analog DSP at RX

Pin-in-hole connectors
- Creates dense via field
  - Disrupts return current
  - Increases high frequency losses
ACI

- **ACI acts as a differentiator:**
  - Pulse signaling
  - Energy per bit reduced
  - Integrate at Receiver

- **ACI acts as a high-pass filter**
  - Compensate for line losses
  - Extends useful frequency range
  - Potentially avoids DSP

- **ACI transformers can be asymmetric**
  - Can accept higher line losses
Why 80% less power dissipation?

Suppose V_{pp}=0.4v, R=50ohm, 6Gbps

For CCI: Power of each pulse is less than \((0.5*(0.2)^2/50)=0.4mw\), totally 5 pulses in period of 10 pulse window, so average power is 0.2mW

For Traditional: Power of each ‘1’ bit is \((0.4)^2/50=3.2mW\), totally 5 ‘1’ bit in period of 10 bit window, so average power is 1.6W

\[ \frac{0.2}{1.6}=0.125, \text{ that is } 87.5\% \text{ less power} \]

For lower frequency switching, even more power saving.
Signal Source: 1 V------Yes
Get into dB too., 9 dB at 1 GHz. ------Now in dB, but why 9 dB at 1GHz????
REDO to just channel response w/- termination artificialities (LL)--------I am simulating what exactly in my design (no termination at RX side, so there is ripples) See backup slides: Wondering: Use Channel_out/IN or Channel_out/Channel_in???
Include sketch of ckt (LL).--------See backup slides
Include measured S12 for capacitor (KC) (or see TEAM report)—included, see next slide
CCI Circuit Schematic

Chip1 TX

Substrate Interconnection TL

Chip2 RX
Kühn's Receiver

Diode Feedback to Set up Local DC level and inhibit unwanted switching due to high frequency noise
Using Latch to recover data

Always high gain.-----added in next slide
Always high Zin? Cm??----see next slide
Noise filter like clamp diode.-----see next slide
Look at frequency response and DC response.-----next slide
What does eye look like at input and why is it opening up?
Not really high freq. noise?—see previous slide
Use this signal for CDR, not input voltage.-----mentioned in slide18
### Codes Evaluated

**4BSB coding**

<table>
<thead>
<tr>
<th>Input word</th>
<th>Output word</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>11110</td>
</tr>
<tr>
<td>0001</td>
<td>01001</td>
</tr>
<tr>
<td>0010</td>
<td>10100</td>
</tr>
<tr>
<td>0011</td>
<td>10101</td>
</tr>
<tr>
<td>0100</td>
<td>01010</td>
</tr>
<tr>
<td>0101</td>
<td>01011</td>
</tr>
<tr>
<td>0110</td>
<td>01110</td>
</tr>
<tr>
<td>0111</td>
<td>01111</td>
</tr>
<tr>
<td>1000</td>
<td>10010</td>
</tr>
<tr>
<td>1001</td>
<td>10011</td>
</tr>
<tr>
<td>1010</td>
<td>10110</td>
</tr>
<tr>
<td>1011</td>
<td>10111</td>
</tr>
<tr>
<td>1100</td>
<td>11010</td>
</tr>
<tr>
<td>1101</td>
<td>11011</td>
</tr>
<tr>
<td>1110</td>
<td>11100</td>
</tr>
<tr>
<td>1111</td>
<td>11101</td>
</tr>
</tbody>
</table>

**5BSB coding**

<table>
<thead>
<tr>
<th>Input word</th>
<th>Output word</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000</td>
<td>101011</td>
</tr>
<tr>
<td>00001</td>
<td>101010</td>
</tr>
<tr>
<td>00010</td>
<td>101001</td>
</tr>
<tr>
<td>00100</td>
<td>101000</td>
</tr>
<tr>
<td>01100</td>
<td>111000</td>
</tr>
<tr>
<td>11100</td>
<td>111001</td>
</tr>
<tr>
<td>11101</td>
<td>111111</td>
</tr>
<tr>
<td>11110</td>
<td>111110</td>
</tr>
<tr>
<td>11111</td>
<td>111110</td>
</tr>
</tbody>
</table>

*Block versions.*

*Above, actually used a “running” version.*
Highest data rate is determined by Jitter and Rising/Falling edge.

Jitter: Caused by ISI, from both coupling cap and Kuhn’s Rx.

Rising & Falling Edge: Determined by Vdd, Device (R & C).

BER: Determined by EYE Opening, jitter of sample clock.

Use this signal for CDR, not input voltage.-----mentioned in slide18
Estimate BER by EYE

Note: Here we assume the signal is gauss distributed.

BER is expressed here by the shadow area:

Blue shadow for BER of ‘1’
Red shadow for BER of ‘0’

BER=Integration of the shadow area
Redo to get 10-17. What NM gives 10-17??----added

Schmidt Trigger RX.-------what do you mean?????
Summary

What are the main factor(s) that cause eye closure?

How is equalization useful?

How are current mode and voltage mode signalling different?

What are the advantages of single-sided TX, differential RX over single-sided RX?
... Summary

What is the advantage of a full differential system?

What are the uses of DC-balanced and run-length codes?

What is the potential advantage of PAM-4 over PAM-2?