Outline

Circuits
- Goals
- Drivers
- Receivers
- On-chip parallel termination
- ESD protection
- On-chip interconnect circuits

References
- D& P, Ch. 11, 7, 8

Goals of Interconnect Circuits

- Achieve good BER under realistic noise conditions, with realistic clocks
- Low power consumption
- Control common mode noise
  - Especially di/dt noise (simultaneous switching noise [SSN])
    - Impacts bit errors in other circuits, as well as this circuit
- Protect chip against electrostatic discharge through pin

E.g. 4-pin TX circuit:
Drivers

Outline:
- Voltage mode drivers
  - Drive and pre-drive
  - Tri-state
  - Rise time control
  - Self-termination
  - Differential
- Current mode drivers
- Transmitter pre-emphasis

Voltage Mode Drivers

Basic Objectives:

- For Vswing > 0.9 Vdd, Rout < 0.1 Z0
  - Large drive transistors
  - Pre-drive circuit needed
    - Remember ratio’d driver (see CMOS notes)
- Must avoid nFET and pFET being on at same time
  - Otherwise large short circuit current during transition
    - Break before Make circuit
- Reasonable area
- Small di/dt
  - Rise time control
Basic Voltage Drivers

Techniques to prevent short-circuit current:

**NAND:** $t_r > t_f$

**NOR:** $t_f > t_r$

Use rise, fall times to prevent $I_{sc}$

(avoid process spread)

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<th>Out</th>
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Reduction of tri-state driver:

*Same functionality as previous page, with fewer transistors and break-before-make*
Rise Time Control

Goal: Reduce \( \frac{di}{dt} \) without significant reduction in delay

- Typically \( tr < 0.3 \sim 0.5 \) \( t_{bit} \)
- Process, temperature variations \( \Rightarrow \) Active control might be desirable (e.g. Use nMOS as pFET and control “resistance”)
- First stage to switch usually the largest

Output Impedance Control

e.g. To precisely match line in series termination

- Digitally trimmed circuit
- NC1, NC2, PC1, PC2 produced by comparing copies of the drive FETs with an off-chip resistor (e.g. voltage division or a bridge)
Differential

Small Swing:

\[ V_{bias} \]

\[ \text{in} \rightarrow \text{out} \]

\[ \text{in}' \rightarrow \text{out}' \]

(Size for a small but finite \( R_{out} \))

Large Swing:

\[ T_{line} \]

\[ \text{IN}_{	ext{POS}} \rightarrow \text{IN}_{	ext{NEG}} \]

\[ \text{OUT} \]

Current Mode Drivers

Single sided:

- Relies on saturated FET

\[ \text{In} \rightarrow \text{Out} \]

Requires:

- \( V_{out} > V_{DD} - V_{t} \)
- Digital trimming to provide \( I_{out} \) across process and temp spreads

Switched Current Mirror

- Series devices must be large
- Small \( V_{G} \) on mirror to max \( V_{sw} \)

Gated Current Mirror

- Smaller devices
- Slower transient response
**Differential Current Mode TX**

Current Steering Circuits:
- Stage 1: Converts large swing to small swing
  - Eliminates dead band at ends of swing in stage 2

**Bipolar Current Mode TX**

Above Unipolar
- Levels: 0 and ±x mA
Create bipolar with complementary pull-up of above
- Logic levels = ±x mA

Example:
Rise Time Control

Can be achieved as per Voltage Mode TX
- Segment drive transistors connected to In (or g) and stagger their turn-on as before

Pre-Emphasis

Simple digital z-domain high pass filter
- Must ensure proper voltage swing

E.g. 2-tap FIR

\[ H(z) = a_0 + a_1 z^{-1} \]
\[ r = -a_1 / a_0 \]
\[ H(z) = a_0 (1 - rz^{-1}) \]
\[ H(w) = a_0 (1 - re^{iw}) \]
\[ |H(\omega)| = |a_0 (1 + r^2 - 2r \cos(\omega))^{0.5} | \]
\[ |H(\omega=0)| = |a_0 (1 - r)| = |a_0 + a_1| \]
\[ |H(\omega=\pi)| = |a_0 (1 + r)| = |a_0 - a_1| \]
Boost = \( (a_0 - a_1) / (a_0 + a_1) = (1 + r) / (1 - r) \)

HPF if \( a_0 > 0 \), and \( a_1 < 0 \)
Current-Mode Pre-Emphasis Circuit

2-tap filter

\[ |a_0| + |a_1| \Rightarrow I_{sw\_max} \]

Voltage Mode Pre-emphasis

Tap weights effectively set by transistor sizes:
- a1 tap smaller transistors than a0 tap
**Receivers**

- Basics on detection and sampling
- Inverters
- Differential
- Clocked differential receivers
  - Integrating
  - Matched filter

**Detection & Sampling**

Eye requirements at input to RX:

- To meet requirements to sample and amplify signal in presence of noise, timing skew and jitter

\[
\text{skew+jitter} \quad \text{aperture time} = t_{\text{setup}} + t_{\text{hold}} - t_r
\]

Why? aperture time = \( t_{\text{setup}} + t_{\text{hold}} - t_r \)

As \( t_{\text{setup}}, t_{\text{hold}} \) measured to 50% points, aperture at top & bottom of eye (at 10%, 90% points)
Detection & Sampling

Alternatives
- Separate amplifier + sampler (i.e., Flip-flop)
- Clocked amplifier (integrated)

Advantages of clocked amplifier
- Lower power
- Jitter contribution of amplifier “portion” reduced
- More sensitivity
- Sampling rate not constrained by gain-bandwidth product

Static (separate) Amplifiers

Inverters
- Gain around $V_{inv} \approx 4/( (V_{GS}-V_{t})(\lambda p + \lambda n))$
- Gain $\approx 20$ for “book” 0.35 $\mu m$ process
- $\Rightarrow$ Sensitivity $\approx (V_{IH}-V_{IL})/\text{Gain} = 2.5/20 = 125$ mV
- Offset determined variation in $V_{inv}$ with process, temp and $V_{dd}$ variations
  - About 300 mV for process variation
  - About 500 mV including temp & $V_{dd}$ variation
- Not best used for initial gain stage in RX
- Useful for final gain stage, however

Inverter Variation
- Schmidt Trigger
  - Hysteresis $\Rightarrow$ very wide NM
Static Differential Receivers

Advantages:

- More sensitive
  - Determined by $g_m$ of source coupled pair and $R_\Delta$ of load
  - 20 – 100 mV
- Less offset voltage
  - Determined by nFET, pFET mismatch
  - 10 mV

Self-Biased Differential RX

Self-biased (Chappell) Receiver

- Current source bias
  - Too high $\rightarrow$ pull input devices out of saturation
  - Too low $\rightarrow$ limits output swing
  - $\Rightarrow$ Self-bias against temp, process variation

Symetric Chappell Amplifier

High input range amp
**Clocked Differential Amplifiers**

See earlier section on differential flip-flops

**Integrating Amplifier**
- Integrator acts like a low-pass filter rejecting high frequency noise

**Matched Filter Amplifier**

Match bias current with shape of Vin
- Matched Filter
On-chip Termination

Binary-weighted trim resistors

- Set trim bits through comparison of a reference circuit with an off-chip resistor