ESD Protection

Static electricity caused by human and machine handling of ICs

• Human body model:

  \[
  1000-5000 \text{ V} \quad 100\text{pF} \quad 1\text{pF} \quad 1.5k\Omega \quad 1\text{pF} \quad 10\text{pF}
  \]

• Effects of ESD
  
  • Breakdown of gate oxide (at $7 \times 10^8 \text{ V/m}$)
    
    ◆ “First breakdown” (not necessarily destructive)
    ◆ 4.9 V for 7 nm thick gate oxide
    ◆ 350 V for 0.5 µm thick field oxide
  
  • Thermal runaway due to high IDS
    
    ◆ “second breakdown” (destructive)
  
  • Avalanche and Zener breakdown in parasitic diode
ESD Protection Circuits

Overall structure

Primary shunt (to ESD “supply”)

- Primary shunt
  - Goal: to drain current to neighboring input pad through ESD supply
  - Use parasitic diode, FET (using field oxide) or transistor
- R: Low-pass filter. Can be an L, at expense of increased area
  - Use poly or diffusion resistor
- Secondary shunt
  - Goal: Voltage clamping: diode-connected nFET

- Note: Adds ~1 pF of capacitance to input
**On-chip Interconnect**

**Distributed RC lines**

\[ \text{trise} \approx 2.2 \text{Rout} (\text{Cout} + \text{Cwire} + \text{CL}) + 0.9 \text{Rwire} \text{Cwire} + 2.2 \text{Rwire} \text{CL} \]

\[ T_{\text{delay}} \approx 0.7 \text{Rout}(\text{Cout} + \text{Cwire} + \text{CL}) + 0.4 \text{Rwire} \text{Cwire} + 0.7 \text{Rwire} \text{CL} \]

- For long wires, delay \( \propto l^2 \)
  - ➔ Use repeaters to reduce delay as \( 2(l/2)^2 < l^2 \)
- Delay with repeater:
  \[ t_d = \left( l/l_s \right) (t_b + 0.4 l^2 \text{RC}) \]
  where \( l = \text{line length} \), \( l_s = \text{segment length} \), \( \text{RC} = \text{per unit length RC} \), \( t_b = \text{buffer delay} \)
**RC lines**

**Optimal Repeater section length**

\[ l_s = \left( \frac{t_b}{0.4RC} \right)^{1/2} \]

Gives delay per unit length

\[ v = 1.3 \left( \frac{t_b RC}{1} \right)^{-1/2} \]

- For 0.35 mm process
  \[ l_s = 3.5 \text{ mm}, \quad v = 17.5 \text{ mm/ns} \]

**Line geometry**

- Increasing line width and spacing reduces RC per unit length
  - Until proximity effect kicks in

**Can use overdrive to compensate for RC loss**

- I.e. Equalization through wave shaping
  - Requires small swing signalling
  - Gives ~ 10% delay improvement
  - Increases Xtalk
  - Ckt overhead

![Diagram of signal waveform with overdrive](image)
Repeater Explosion!

From ITRS:

- In practice sub-optimal repeater insertion used

\[ W = S = 2P_m \]
\[ L_{\text{max}} = (310)^{1/2} \text{ mm} \]
2 adj. lines
Voltage vs. Current Sensing

Current Sensing
- Low impedance termination

\[ R_L \approx 0 \]

Voltage Sensing
- High impedance term. (i.e. capacitive)

\[ R_L \approx \infty \]

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\( C_{\text{INT}} \)
\( R_{\text{INT}} \)

\( L \)
\( C \)
\( Z \)
\( \omega \)
\( \beta \)
\( V_{\text{out}} \)
\( R_{\text{in}} \)

\( \beta \)

\( V_F \)
\( A_V \)
\( Z_0 \)
\( R_F \)

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Current Mode Delay Analysis

\[ V_{IN} \]

Interconnect RC (ns)

Delay (ns)

- distributed (N=1000)
- this work
- Sakurai’s model

Interconnect RC (ns)

Delay (ns)

- distributed (N=1000)
- this work
On-chip Current Mode Signalling

Decreased delay

Why?

Voltage Mode

\[ \tau = R_O C_L \]

Current Mode

\[ \tau = \frac{R_L R_O C_L}{R_L + R_O} \]

Impact:

- Fewer repeaters
- Narrower wires

At expense of DC power consumption
**LRC lines**

Can “tune” line

- Critically damped (or slightly underdamped in practice) gives min delay, rise time

Again, can equalize line to get optimum response

- FIR
- Wave-shaping
- Key: Simple circuits
Summary

Drivers require large transistor. What is important to avoid?

Large drivers $\rightarrow$ large $\text{di/dt}$. How to reduce?

What are the advantages of current mode drivers?

What determines eye opening at Rx?
Summary

How can delay be minimized in on-chip lines?