ESD Protection

Static electricity caused by human and machine handling of ICs

• Human body model:

  \[ 1000-5000 \text{ V} \]

  \[ 5\mu H \]

  \[ 1pF \]

  \[ 1.5k \Omega \]

  \[ 100\text{pF} \]

  \[ 10\text{pF} \]

• Effects of ESD

  • Breakdown of gate oxide (at \(7 \times 10^8 \text{ V/m}\))
    - “First breakdown” (not necessarily destructive)
    - 4.9 V for 7 nm thick gate oxide
    - 350 V for 0.5 \(\mu\)m thick field oxide
  
  • Thermal runaway due to high IDS
    - “second breakdown” (destructive)
  
  • Avalanche and Zener breakdown in parasitic diode

ESD Protection Circuits

Overall structure

Primary shunt
(to ESD “supply”)

Secondary shunt (to normal supply)

• Primary shunt
  - Goal: to drain current to neighboring input pad through ESD supply
  - Use parasitic diode, FET (using field oxide) or transistor
  - R: Low-pass filter. Can be an L, at expense of increased area
    - Use poly or diffusion resistor

• Secondary shunt
  - Goal: Voltage clamping: diode-connected nFET

• Note: Adds ~1 pF of capacitance to input
**On-chip Interconnect**

Distributed RC lines

\[ \text{trise} = 2.2 \frac{R_{out}}{R_{wire}} (C_{out} + C_{wire} + CL) + 0.9 R_{wire} C_{wire} + 2.2 R_{wire} CL \]

\[ \text{Tdelay} = 0.7 \frac{R_{out}}{R_{wire}} (C_{out} + C_{wire} + CL) + 0.4 R_{wire} C_{wire} + 0.7 R_{wire} CL \]

- For long wires, delay \( \propto l^2 \)
- Use repeaters to reduce delay as \( 2(l/2)^2 < l^2 \)
- Delay with repeater:
  \[ t_{d} = \frac{l}{2} (t_{b} + 0.4l^2 RC) \]
  where \( l = \) line length, \( l_s = \) segment length, \( RC = \) per unit length RC, \( t_b = \) buffer delay

**Optimal Repeater section length**

\[ l_s = \left( \frac{t_b}{0.4RC} \right)^{1/2} \]

Gives delay per unit length

\( v = 1.3 \left( \frac{t_b}{R_C} \right)^{1/2} \)

- For 0.35 mm process
  \[ l_s = 3.5 \text{ mm}, \quad v = 17.5 \text{ mm/ns} \]

**Line geometry**

- Increasing line width and spacing reduces RC per unit length
- Until proximity effect kicks in

**Can use overdrive to compensate for RC loss**

- I.e. Equalization through wave shaping
  - Requires small swing signalling
  - Gives \( \sim 10\% \) delay improvement
  - Increases Xtalk
  - Ckt overhead

\[ \begin{array}{c}
V_t \\
1 \\
0 \\
V_t
\end{array} \]
Repeater Explosion!

From ITRS:
- In practice sub-optimal repeater insertion used

\[ W = S = 2P_n \]
\[ L_{	ext{max}} = (310)^{1/2} \text{ mm} \]
2 adj. lines

Voltage vs. Current Sensing

Current Sensing
- Low impedance termination

\[
\begin{align*}
R_I & \quad \text{[Resistor]} \\
C_{\text{INT}} & \quad \text{[Capacitor]} \\
R_L & \approx 0
\end{align*}
\]

Voltage Sensing
- High impedance term. (i.e. capacitive)

\[
\begin{align*}
R_I & \quad \text{[Resistor]} \\
C_{\text{INT}} & \quad \text{[Capacitor]} \\
R_L & \approx \infty
\end{align*}
\]

Voltage-Mode Receiver
\[ Z_L = -j \frac{1}{\omega C_L} \]

Current Mode Receivers
\[ Z_L = -j \frac{1}{\omega C_L} \frac{1}{g_{mN} + g_{mP}} \]
\[ Z_L = -j \frac{1}{\omega C_L} \frac{R_p}{1 + A_B \beta} \]
\[ Z_L = -j \frac{1}{\omega C_L} \frac{Z_o}{1} \]

\[ c/-\text{ Rizwan Bashirullah} \]

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**Current Mode Delay Analysis**

![Diagram showing current mode delay analysis](image)

**On-chip Current Mode Signalling**

Decreased delay

Why?

Voltage Mode

\[ R_O \]

\[ C_L \]

\[ \tau = R_O C_L \]

Current Mode

\[ R_O \]

\[ C_L \]

\[ \tau = \frac{R_I R_O C_L}{R_L + R_O} \]

Impact:

- Fewer repeaters
- Narrower wires

At expense of DC power consumption
LRC lines

Can “tune” line
  - Critically damped (or slightly underdamped in practice) gives min delay, rise time

Again, can equalize line to get optimum response
  - FIR
  - Wave-shaping
  - Key: Simple circuits

Summary

Drivers require large transistor. What is important to avoid?

Large drivers \(\rightarrow\) large \(\frac{di}{dt}\). How to reduce?

What are the advantages of current mode drivers?

What determines eye opening at Rx?
Summary

How can delay be minimized in on-chip lines?