ESD Protection

Static electricity caused by human and machine handling of ICs

- Human body model:

- Effects of ESD
  - Breakdown of gate oxide (at $7 \times 10^9$ V/m)
    - “First breakdown” (not necessarily destructive)
    - 4.9 V for 7 nm thick gate oxide
    - 350 V for 0.5 µm thick field oxide
  - Thermal runaway due to high IDS
    - “second breakdown” (destructive)
  - Avalanche and Zener breakdown in parasitic diode
ESD Protection Circuits

Overall structure

- Primary shunt
  - Goal: to drain current to neighboring input pad through ESD supply
  - Use parasitic diode, FET (using field oxide) or transistor
- R: Low-pass filter. Can be an L, at expense of increased area
  - Use poly or diffusion resistor
- Secondary shunt
  - Goal: Voltage clamping: diode-connected nFET
- Note: Adds ~1 pF of capacitance to input
On-chip Interconnect

Distributed RC lines

\[ \text{trise} = 2.2 \, \text{Rout} \, (\text{Cout} + \text{Cwire} + \text{CL}) + 0.9 \, \text{Rwire} \, \text{Cwire} + 2.2 \, \text{Rwire} \, \text{CL} \]

\[ \text{Tdelay} = 0.7 \, \text{Rout}(\text{Cout}+\text{Cwire}+\text{CL}) + 0.4 \, \text{Rwire}\text{Cwire} + 0.7 \, \text{Rwire} \, \text{CL} \]

- For long wires, delay \( \propto l^2 \)
  - Use repeaters to reduce delay as \( 2(l/2)^2 < l^2 \)
- Delay with repeater:
  \[ t_d = (l/l_s)(t_b + 0.4 l_s^2 RC) \]
  where \( l = \) line length, \( l_s = \) segment length, \( RC = \) per unit length RC, \( t_b = \) buffer delay
**RC lines**

Optimal Repeater section length

\[ l_s = (t_b/0.4RC)^{1/2} \]

Gives delay per unit length

\[ v = 1.3 (t_b RC)^{-1/2} \]

- For 0.35 mm process
  \[ l_s = 3.5 \text{ mm}, v = 17.5 \text{ mm/ns} \]

Line geometry

- Increasing line width and spacing reduces RC per unit length
- Until proximity effect kicks in

Can use overdrive to compensate for RC loss

- I.e. Equalization through wave shaping
  
  - Requires small swing signalling
  - Gives ~ 10% delay improvement
  - Increases Xtalk
  - Ckt overhead
Repeater Explosion!

From ITRS:

- In practice sub-optimal repeater insertion used

\[ W = S = 2P_m \]

\[ L_{\text{max}} = (310)^{1/2} \text{ mm} \]

2 adj. lines

\[ f_{\text{clock}} \]

\[ f_{\text{input}} \]

\[ f_{\text{output}} \]

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<th>Technology Node (nm)</th>
<th>Frequency (GHz)</th>
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<th>Power dissipation (mW)</th>
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<th>Technology Node (nm)</th>
<th>Optical number of repeaters (1/cm)</th>
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<th>Technology Node (nm)</th>
<th>Repeat area (um^2)</th>
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Voltage vs. Current Sensing

Current Sensing
- Low impedance termination

$$RL = 0$$

Voltage Sensing
- High impedance term. (i.e. capacitive)

$$RL = \infty$$

Voltage-Mode Receiver

$$Z_L = -j \frac{1}{\alpha C_L}$$

Current Mode Receivers

$$Z_L = -j \frac{1}{\alpha C_L} \left( \frac{1}{gm_N + gm_P} \right)$$

$$Z_L = -j \frac{1}{\alpha C_L} \frac{R_F}{1 + \beta}$$

$$Z_L = -j \frac{1}{\alpha C_L} \left( Z_o \right)$$

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Rizwan Bashirullah
Current Mode Delay Analysis
On-chip Current Mode Signalling

Decreased delay
Why?

Voltage Mode
\[ R_O \rightarrow C_L \]
\[ \tau = R_O C_L \]

Current Mode
\[ R_O \rightarrow C_L \rightarrow R_L \]
\[ \tau = R_L R_O C_L / (R_L + R_O) \]

Impact:
- Fewer repeaters
- Narrower wires

At expense of DC power consumption
**LRC lines**

Can “tune” line
- Critically damped (or slightly underdamped in practice) gives min delay, rise time

Again, can equalize line to get optimum response
- FIR
- Wave-shaping
- Key: Simple circuits
Summary

Drivers require large transistor. What is important to avoid?

Large drivers \(\Rightarrow\) large di/dt. How to reduce?

What are the advantages of current mode drivers?

What determines eye opening at Rx?
Summary

How can delay be minimized in on-chip lines?