Timing

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Outline
1. Clock distribution
2. Standard single-phase, single-clock design
3. Two phase design styles

References
- Doane & Franzon, “Multichip Module Technologies & Alternatives”, CH. 11
- Hodges & Jackson, Analysis & Design of Digital Integrated Circuits
- + many other texts
Clock Distribution

Goal: Distribute master clock with identical clock edge arrival times at flip-flops or latches

Problem:
- Clock (capacitive) load is large
- Clock load is not evenly distributed on the chip

“Standard” Solutions
- Clock Trees (most ICs)
- Clock Grid (some microProcessors)
- Sepertines (some microProcessors and some small high speed circuits)

Measures of clock distribution quality
- Worst-case skew
  - systematic variation in space
- Jitter
  - random variation in time (cycle to cycle edge movement)
- Clock edge rate
**H-tree Clock Layout**

Standard Technique for Low-Skew clock distribution

- **Objective**: Identical delay to all flip-flops from source
- **Methods**:
  - Balance RC delays along all paths
  - Can be difficult as Cload not uniformly distributed
  - Rebuffer to increase edge rate at local level

![Diagram of H-tree clock layout](local rebuffer to sharpen edge rate)
Other Layouts

Clock Grid:
- Low (but none zero) skew
- Easy to design
- Higher power
- Can be used to replace first layers of tree

Serpentine
- Again trades ease of design for higher power
- Point to point wires
  - Identical delay
Clock Skew

Skew due to differential delays:

- Skew = systematic variation
  - Varied buffer delays
  - Wiring delay differences

Jitter = cycle to cycle variation at any one point
- Phase lock loop noise
  - caused by noise in Vdd/Gnd
- Varying trigger points at buffer
- Environmental effects
- Seen as “fuzz” in eye diagram
Single Phase Clock with Master-Slave Flip-Flops

Best used with Static Logic, as no precharge period available.

Minimum Clock Period:

- $t_{clock}$
- To revent 'setup violations'

$$t_{clock} = t_{flip-flop-max} + t_{logic-max} + t_{interconnect-max} + t_{setup-max} + t_{skew-max} + t_{jitter-max}$$

![Diagram of clock and flip-flop connections with timing labels](image-url)
...Timing Equations

Requirement to Prevent Race:

- Prevents 'hold violations'

\[ t_{\text{hold-max}} < t_{\text{flip-flop-min}} + t_{\text{logic-min}} + t_{\text{skew-max}} + t_{\text{interconnect-min}} \]

Diagram:

- Logic + Interconnect
- Clock-1 to Clock-2
- Notionally same, random skew
- T_{skew+jitter-max}
- T_{hold-max}
- T_{flip-flop-min}
- T_{logic-min} + T_{interconnect-min}
Single Phase Latch Design

Structure:

- Requires two types of latches (n and p)
- Not seen much in practice
**Two Phase Clocking**

Locally generate clock’ from clock.

Nominal timing relationships

“Slack Borrowing”: Up to half a clock cycle of extra logic delay can be accumulated in the pipeline.
Two Phase with Dynamic Logic

Nominal timing relationships

"Slack Borrowing": Can adjust timing by trading logic delay before and after latch.

e.g. \( tS1b \) can be reduced, so as to increase \( tS2a \) and put more logic in \( S2a \) and \( S2b \) combined.
**Time Stealing**

Locally move clock edges.

![Diagram of time stealing](image)
Variations on these Schemes

Variations:
- Underlapped two-phase clocks to account for local clock skew
- Time stealing with static logic and Master-slave flip-flops
- Logic with feedback
  - Requires that feedback structure looks like the pipeline
  - e.g. a sequence of a pair of latches
  - Take care in timing rules