10 MB/S TWISTED PAIR CMOS TRANSCEIVER WITH TRANSMIT WAVEFORM PRE-EQUALIZATION

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Abstract
A 5-volt CMOS 10MB/S transceiver as the Media Access Unit (MAU) for the unshielded twisted pair 10Base-T Ethernet is described. The internal differential delay line loop can track incoming 20MHz ± 40% reference with measured jitter less than ± 0.55 ns. A dual level rail-to-rail Manchester code line driver is employed. With random data input, both the receive and transmit circuits induce less than ± 1.2ns and ± 1.7ns jitter respectively.

Introduction
Traditionally, the Ethernet network is carried through expensive coaxial cable. Recently, unshielded twisted pair (UTP) media has been standardized as an alternate media that is cheaper and more readily available for a 10Mb/s Ethernet network (10Base-T).

A simplified block diagram of the 10Mb/s transceiver is shown in Fig. 1. Because of the narrower bandwidth of UTP compared to coaxial cable, the Manchester code transmitted on the UTP needs to be pre-equalized at the transmit side to minimize intersymbol interference. The Ethernet network has a tight jitter budget to ensure reliable data recovery[1]. The allowable jitter on the MAU section is another major design issue of this chip.

Transmit Section
The transmit predistortion is accomplished by reducing the pulse height of the second half of the Manchester wide pulse. A predistored output waveform to the twisted pair transmit filter is shown in Fig. 2. An internal half bit time delay generator is needed to accomplish the predistortion. For symmetrical rise/fall time and jitter performance, a fully differential structure is used in most critical paths. In the delay generator, a differential pair stage with a self calibrated load is used as the basic delay element (Fig. 3). The delay of each delay element is determined by the bias current, the voltage swing and load capacitance. The reference delay loop is designed to have a ± 30% pull range to account for temperature and process variations. Instead of changing the delay by controlling the swing voltage amplitude[2], a supply current adjustment is chosen for wider center frequency variation range.

Fig. 1 Simplified 10Mbit/s twisted pair transceiver block diagram

Fig. 2 The twisted pair transceiver output after the transmit filter. The pulse height is reduced at the second half of the Manchester wide pulse

7.3.1
Fig. 3 Simplified reference delay line with control circuit schematic

For low jitter consideration, a phase detector with added phase difference is used that allows the charge pump current source to resolve small phase differences during in-lock condition. With the added phase difference, it also allows use of a smaller current source to reduce the loop bandwidth without using large external capacitor. A + - 0.55ns worst case jitter performance is achieved with on-chip loop filter where the integration capacitor value is only 10pF.

The line driver is a rail-to-rail dual level voltage driver that is feeding the transmit filter and the following twisted-pair transformer and line through two 48 Ohm termination resistors. A simplified schematic of the line driver is shown in Fig. 4. The line driver is operating in two different modes. The digital full swing mode where the output swing reaches VCC - Vdsat is designed for the provision of the fullstep voltage. The analog voltage follower mode is designed to provide the reduced pulse height in the second half of the wide pulse.

In the digital full swing mode the circuitry can easily be described with the function of a simple inverter. In the analog mode an operational amplifier is provided with 2.75V as a halfstep reference voltage. This voltage level is then replicated at the source of a reference NMOS device and held constant through the help of the high speed opamp. The gate voltage of the reference NMOS device is then given to a large NMOS driver device. The current in the path and the device size are scaled accordingly. The source voltage under the scaled operating conditions is then approximately the same as the reference voltage. This methodology provides an almost ideal behavior at the output, with a clean predistortion of the signal necessary for feeding the 5th-order Cauer-Parameter transmit filter.

Fig. 4 The rail-to-rail, dual level line driver simplified schematic

**Receive Section**

The receive section of the chip receives filtered data from the twisted pair. Due to the Ethernet system requirement, a low jitter slicer, a highly efficient bridge type driver and a squelch circuit with adjustable squelch level are used in the receiver section.

The squelch circuit has a differential input stage with a built-in squelch voltage and a high gain stage to convert the input level to CMOS logic level. A differential source follower with poly resistor inserted between the NMOS device and the current source is used to generate the squelch level. Because the bias current is generated from the on chip resistor, the threshold level only depends on resistor matching. The threshold voltage can be adjusted by changing the bias current. Squelch levels of both polarity are available by selecting appropriate taps across the differential source follower structure (Fig. 5).

Fig. 5 The simplified squelch circuit schematic
In the data ailer, a MOS diode structure is added to prevent the differential stage active load from going into the triode region. This clamp diode improves the speed of the comparator while maintaining high gain and lower sensitivity to the next stage offset and allows a combination of high gain and high bandwidth in one stage.

**Experimental Results**

Using a 100 meter (maximum specified distance) unshielded twisted pair, the transceivers are successfully tested for information exchange without error. The experimental results show the pre-distorted transmit pulse after the line model fits into the pulse template provided by the 10Base-T standard (Fig. 6). The 10Base-T link integrity pulse is also generated with the same driver structure and the pulse fits into the template as shown in Fig. 7. The transmit jitter is within the specification. In test mode, the delay line reference loop performance is measured being able to track incoming 20MHz +/− 40% with jitter no more than +/− 0.55ns (shown in Fig. 8) from 10 randomly chosen samples. The transmit and receive jitter are measured on an eye diagram with a worst case random data pattern as input. Due to the differential structure and process insensitive design, the receive circuit induced jitter is less than +/− 1.2ns and the transmit circuit induced jitter is less than +/− 1.7ns over all supply voltages (4.7V−5.3V) and temperatures (−10−85 °C).

Using a single poly, double metal 2 micron technology, the die size is 190 x 216 sq mil and the die photo is shown in Fig. 9. The power consumption is 250mW while the line is idle and 550mW while it is in external loopback configuration and continuously transmitting an all-one pattern (worst case power condition).

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Fig. 6 The worst case random data transmit waveform after the line model vs. the 10Base-T pulse template

Fig. 7 The link integrity pulse waveform before the line with the 10Base-T link pulse template

Fig. 8 The delay line loop clock output with the lower trace as the enlarge signal for jitter measurement.
Fig. 9 The die photo of the 10Mbit/s twisted pair CMOS transceiver

References

[1] IEEE 802.3 10Base-T standard Draft 12