Optimization of DRAM Sense Amplifiers for the Gigabit Era

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Abstract: This paper reviews sense amplifier design challenges as DRAM densities are increased beyond a gigabit. Various proposed solutions for maintaining high performance and sensitivity, while reducing the array voltage are reviewed. Pre-amplification, body-effect control, Vt mismatch cancellation, and two revolutionary solutions are presented and discussed.

I. INTRODUCTION

The sense amplifier (SA) is perhaps the most critical circuit in a DRAM chip. It must reliably detect and amplify the small (<100mV) differential signal that appears on the bitlines following charge transfer from the storage cell capacitor. After this destructive read, the SA must restore the proper voltage back into the storage capacitor. SA's must have high sensitivity, high performance, small area, and must match the tight layout pitch of the cell array.

The simple cross-coupled type SA was introduced and optimized for NMOS DRAMs in the 1970's [1,2] and then for CMOS DRAMs in the 1980's [9-11]. The typical CMOS sense amplifier circuit (Fig. 1) consists of three NFETs next to each array block to equalize and precharge the bitlines to Vcc/2, cross-coupled NFET and PFET sense latches to drive the bitlines to GND and Vcc, two NFETs to transfer amplified data to the I/O lines, and a set of NFET isolator/MUX devices on each side of the sense amplifier. These isolator devices, placed between the sense nodes and the bitlines, serve two purposes: 1) to permit the SA to be shared between adjacent array blocks, and 2) to isolate the sense nodes from the heavily loaded bitlines, thereby improving sensing performance. For maximum sensitivity, it is essential that SA offset voltage be minimized. This offset voltage is caused by Vt mismatch between the cross-coupled latch devices, and is amplified by gm and sense node capacitance imbalances.

II. SENSE AMPLIFIER DESIGN PROBLEMS & SOLUTIONS

As DRAM densities enter the gigabit era, there are three key SA design issues that must be resolved: 1) maintaining high performance despite decreasing array Vcc, 2) maintaining sufficient sensitivity despite the increasing effect of SA imbalances, and 3) reducing the chip area consumed by SA's despite the increasing number of SA's per chip.

A. Effect of Array Voltage Reduction

The Vcc/2 precharge level minimizes power dissipation and noise generation due to charge sharing and symmetrical voltage swings. However, to further reduce power and maintain device reliability, the array voltage (VCC) will be scaled to 1.5V and below. This severely degrades the sensing performance, because the threshold voltage of the sense latch devices cannot be scaled as rapidly as Vcc and still maintain sensing margin. Several good solutions have recently been proposed.

B. Pre-amplification Techniques

The first charge-transfer SA was designed for NMOS DRAMs with the bitlines precharged to GND.[3,4] However, this approach is not directly extensible to VCC/2 CMOS DRAMs. Recently, a charge-transfer pre-sensing scheme (CTPS) [26] has demonstrated a 40% increase in sensing speed with a 5X signal preamplification at an array VCC of only 0.8V. This scheme (Fig. 2) precharges the sense nodes to 2VCC = 1.6V and the bitlines to VCC/2 = 0.4V. After initial signal development on the bitlines, the isolator devices turn on, back-transferring charge from the sense nodes to the bitlines. This inverts the bitline signal on the sense nodes and preamplifies the original signal by the ratio (Cn + Cs)/Cs. The sensing that follows is faster due to the larger signal and to the large overdrive on the NMOS latch. This speeds up a normal read, but the full refresh writeback time is degraded to 95ns. Also, this technique is actually slower than conventional sensing for VCC>1.2V.

Another preamplification technique uses bootstrap capacitors to boost the sense nodes to a higher voltage prior to sensing [6]. As in the previous technique, this has the combined effect of increasing the SA overdrive and preamplifying the signal. The charge-amplifying boosted sense (CABS) scheme [28] (Fig. 3) uses voltage-dependent MOS capacitors for boosting the sense nodes, which preamplifies the initial signal while the sense nodes are temporarily isolated from the bitlines. The difference in charge transferred to the two sense nodes (the preamplification factor) increases with both Vcc and the size of the boost capacitors. Sensing speed is improved by 70% and the signal margin by 30% at VCC=1.5V and Cp=20F. However, some of this advantage is lost due to mismatches in the boost capacitors, which require extra area and careful layout.

C. Dynamic Body-Bias Control

Sensing begins when the sense line SAN drops to a Vt below the VCC/2 precharge level of the sense nodes. The p-well of the NFET latch is typically biased at GND, which unfortunately increases the latch Vt due to the body-effect. This, in turn, delays the onset and speed of sensing. Recent SA designs have featured dynamic control of isolated wells containing the latch devices. This requires either a triple-well or SOI process for proper isolation of both N & P-wells. The charge transfer well (CTW) scheme [22] (Fig. 4) employs charge sharing between the VCC/2 set nodes and their
respective wells at the onset of sensing. This temporarily reduces $V_{BS}$ of the latch devices, lowering their $V_t$, and improving sensing time by 19%. This charge-sharing approach to control the body-biases does not draw any additional current from the power supplies.

Body-synchronous and Super Body-synchronous sensing schemes [15, 24] dynamically switch the latch device wells synchronously with the sense lines to yield zero body-effect and negative body-effect, respectively [Fig. 5]. However, there is significant parasitic capacitance associated with these wells, which prevents faster switching and leads to higher power dissipation. This problem is alleviated in SOI DRAMs [24] where the dielectrically-isolated body has a greatly reduced capacitance, and can be switched with low power dissipation.

D. Threshold Voltage Mismatch Compensation

The maximum number of cells that can be connected to a SA is limited by SER and the SA offset. Therefore, as DRAM density increases, the number of SA’s per chip is also increasing to over one million on a 1Gb chip! This implies that for a given $V_{t}$ distribution, a larger number of standard deviations ($\sigma$) must be tolerated for each DRAM generation. In addition, as the SA devices shrink, the short channel effect tends to widen the $V_{t}$ distribution further [12-14,19,20]. This growing problem has led to several designs to compensate for $V_{t}$ mismatch. The first proposals [5,7,8,17] worked by adjusting the bitline precharge levels to $\Delta V_{t}$ through transfer devices biased near threshold, so the operation was rather slow. This can be accomplished by using both local (D) and global (GD) bitlines, “direct” sensing (drains of sense devices connected directly to I/O lines instead of cross-coupled), and two new switches to diode-connect the sense transistors and compensate for their $V_{t}$ mismatch [17]. In another approach, a current-mirror differential amplifier is added between the bitlines and N-latch [18][Fig. 6]. This is called the offset-compensating scheme (OCS), and is different in that it cancels all the electrical imbalances. It achieves faster signal development and sensing, but increases the SA area by 70% due to the large current-mirror amplifier. Recently, an offset-trimming scheme with both high speed and small area, using the direct sensing scheme has been proposed [25] [Fig. 7]. This SA effectively consists of two inverters with feedback switches which are closed during the trimming period, eliminating the offset voltage. During sensing the feedback path is broken and the inverters are connected to the I/O lines. The performance is improved by 50% over an uncompensated SA for a 50mV offset, and the area penalty is only 13%.

E. Revolutionary Solutions: Gain Cells & Multi-level Sensing

Conventional charge transfer 1-T DRAM cells are severely limited in the number of cells per SA (only 128-256). Several 2-T “gain” cells have recently been proposed to alleviate this constraint. A good example is the SGT cell [16] [Fig. 8], where reading the cell causes a current to flow from the bitline to a power supply. This implies that the SA’s role is limited to detecting and transmitting this small, differential signal to the I/O path. There is no need for the SA to amplify the signals to full CMOS levels, thus improving speed. The SA becomes an analog differential amplifier. Therefore, the number of cells attached to this SA can be greatly increased, reducing the area of SA’s on the chip.

Another novel approach to increasing DRAM density is 4-level storage [27], effectively doubling the density of the DRAM array. However, to reliably resolve and latch four different voltage levels places extremely tight constraints on the sense amplifier. Charge coupling sensing and charge sharing restore are used to detect these small [Fig. 9].

III. CONCLUSIONS

A number of potentially useful solutions dealing with the problems of SA performance at low $V_{CC}$, $V_{t}$ mismatch, and layout area have been identified. These concepts will need to be combined and/or enhanced to enable reliable sub-1.5V sensing in multi-gigabit DRAMs of the future.

REFERENCES


Fig. 1 Typical CMOS sense amplifier and its waveforms [Ref. 23]

Fig. 2 Charge-transfer pre-sensing (CTPS) scheme with 40% faster sensing at Vcc=0.8V [Ref. 26]

Fig. 3 Charge-amplifying boosted sense (CABS) scheme with MOS boost capacitors on sense nodes. [Ref. 28]

Fig. 4 Charge-transfer well (CTW) scheme. Sense nodes and their bodies are partially equalized through SOF devices. [Ref. 22]
Super body-synchronous sensing scheme.

Fig. 5 Super body-synchronous switching of the sense latch bodies lowers their $V_t$ to 0.35V in the sensing state. [Ref. 24]

Operation modes of SGT cell: (a) write mode, (b) read mode.

Fig. 8 Surround Gate Transistor (SGT) Gain cell. The SA is designed to detect a small read current on the bitline. [Ref. 16]

Charge Sharing Restore Scheme

<table>
<thead>
<tr>
<th>Restore Level</th>
<th>MSB</th>
<th>Vrestore</th>
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<tbody>
<tr>
<td>LSB 1</td>
<td>Vcc</td>
<td>$\frac{3}{2}$ Vcc + CB + $\frac{1}{3}$ CB</td>
</tr>
<tr>
<td>LSB 0</td>
<td>0</td>
<td>0 (GND)</td>
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Charge Coupling Sensing

Fig. 9 4-Level storage scheme for multi-gigabit DRAM [Ref. 27]