840 Mb/s CMOS Demultiplexed Equalizing Transceiver for DRAM-to-Processor Communication

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ABSTRACT

An equalizing transceiver was designed for DRAM bus system and implemented using a 0.35 \mu m CMOS technology. To maximize the data rate a one-to-eight demultiplexing scheme was used to remove inter-symbol interference. The maximum data rates were measured to be 840 Mb/s without loading and 760 Mb/s with the total capacitance load of 110 pF at the bit error rate less than 10^{-12}. The chip size was 1500\times700 \mu m^2 and the power consumption was 150 mW at the supply voltage of 3.3 V.

Introduction

In DRAM bus systems, the total capacitance loading on a data bus can be more than 100 pF due to the parasitic capacitance of DRAM I/O pins. The data bus behaves similarly to a distributed RC channel due to the parasitic capacitances and the characteristic impedance of transmission line. Fig. 1 illustrates the principle of equalization. A pulse of width T is transmitted through a band-limited RC channel. The transient response does not decay to zero at t\approx2T due to the limited bandwidth. To remove ISI(inter-symbol interference), \alpha times the value at t\approx T should be subtracted from the value at t=2T.

Recently, equalization[1] and PRD(partial response detection)[2] schemes were proposed to remove the ISI component. Since the ISI subtraction circuits in previous works should complete the equalization operation during a single[1] or two data periods [2], it is expected that the ISI subtraction circuit be a bottleneck in increasing the data rate.

Architecture

In this work, a synchronous bus system was assumed. The clock skew due to the difference in path delay[3] was eliminated by matching the length of clock and data flow paths as shown in Fig. 2. The data from CPU to DRAMs are synchronized with ClkFromMaster. Similarly, the data from DRAM to CPU are synchronized with ClkToMaster. In this work, the frequency of external clocks(ClkFromMaster and ClkToMaster) is set to one-eighth the data rate.

Fig. 3 shows the block diagram of the transceiver proposed in this work. As an example, the data rate is assumed to be 1 Gb/s and the external clocks(ClkToMaster and ClkFromMaster) are set to be 125 MHz which is one-eighth the data rate. The transmitter part includes an eight-times frequency-multiplying PLL and an output driver. The receiver part includes a regular PLL, an eight-times frequency-multiplying PLL, an equalizer block, and an eight-to-one multiplexer. The regular PLL generates eight 125 MHz clocks which have eight different phases with the phase separation of 45°. The equalizer block includes eight equalizers operating in parallel at the clock frequency of 125 MHz. The outputs of eight parallel equalizers are serialized by the eight-to-one multiplexor.

Circuit Description

Fig. 4 shows the circuit schematic of the equalizer used in the receiver. V_l(n) and V_l(n-1) represent the input voltages sampled at a rising edge and the preceding rising edge of the 1 GHz clock respectively. V_RF represents the reference voltage and corresponds to the average value of the two NRZ(non-return-to zero) signal levels. The eight transistors(M1-M8) constitute the ISI subtraction circuit. If the W/L values of M3 and M4 are designed to be \alpha times those of M1 and M2, the drain current through M8 can be represented by

\[ I_{DS} = g_m \cdot \{ V_l(n) - \alpha \cdot V_l(n-1) \} \]  

(1)

The ISI-free results(Vo+) and Vo-) are latched at the O+ and O- nodes in CMOS logic level by the latch circuit(M11-M19).

To allow enough time margin for the equalizer operation, eight equalizers are used in parallel as shown in Fig. 5. The eight clocks(\phi_1-\phi_4, \phi_1-\phi_4) for the equalizers are generated by the regular PLL in the receiver. In this way, each equalizer has eight data periods(8T) to process a bit of data. Hence the equalizers of this work do not impose the speed bottleneck in maximizing the data rate.

Measurements

The test chip was implemented by using a 0.35 \mu m four-metal double-poly N-well CMOS technology. The chip size was 1500\times700 \mu m^2 excluding the pad area. To emulate the loading of DRAM I/O pins, 5 pF-capacitors were deliberately attached to the transmission line on the test board in uniform spacing(2 cm) between the data bus and the ground plane and also between the clock line and the ground plane. On the test board two test chips corresponding to transmitter and receiver were attached at both ends of the transmission lines which were
terminated by 50 Ω resistors. Throughout all the measurements of this work, the test criterion of BER(bit error rate) for successive data transmission was set to be 10⁻¹². The maximum data rate was measured to be 840 Mb/s, when the data was transmitted over a short link with no capacitance added deliberately. When twenty-two 5pF-capacitors were connected on the PCB transmission lines between the transmitter and the receiver on each transmission line, the maximum operating speed of the receiver was measured to be 760 Mb/s. The measured eye diagram on the receiver I/O pin is shown in Fig. 6. From this band-limited signal the equalizer recovered the original transmitted data. The partial response ratio, α, was chosen to be 1/3 in this work.

References