Question 1 [20 points]
Consider the flip-flop below.
Please answer the following questions:

(a) Please complete the following waveforms. Used a dashed line for when a node is floating in a certain condition. [6 points]

(b) Explain explicitly what happens around time 1. Specifically give the states of all transistors before and after the clock edge – focus on the sampling event. [4 points]

(c) What happens at time 2 – why does the FF state not change? What prevents floating nodes? [2 points]
(d) Which flip-flop style in class is this closest to? [2 points]

(e) How is it significantly different than the flip-flops in class? [2 points]

(f) Why don’t we need a full inverter pair at the Q outputs? [2 points]

(g) What style of dynamic logic is this flip-flop best suited to? Why? [2 points]