ECE 520/492B / DS 510P: Homework 3

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Due Date: Friday, March 27
(Off-campus students: One week later)

Total Points: 80

Question 1
Do tutorial 2 in the class locker (tutorials/tutor2). Then do the following design exercises:

a. Redesign the Mealy machine used in the tutorial so that its outputs are registered. Synthesize the machine. Turn in your Verilog, your ‘simmax’ simulation vectors and schematics of the final design (as plotted from Synopsys). Please comment on the following:

i. How is the final design different in timing and behavior than the original design?
ii. Is there any hierarchy in the final design?

Question 2
Do question 3 from the 1999 mid-term:

Redesign the drag race lights example so that it is actually a traffic light controller. Its behavior is to be that it is normally red. When a car comes along ('car'==1), it goes green for 200 clock cycles, then yellow for 10 clock cycles, and then back to red. Clearly show the structure of your design, as well as the Verilog.

Structure your solution as two modules - an FSM and a counter. Use the structured synthesis approach discussed in the current set of notes ('characterize'). Turn in a sketch of your design, your Verilog, a simulation of your design, your synthesis script, and a schematic of the final design. [20 points]
(You are NOT required to do FSM optimization for this question.)

Question 3
Turn in what you consider to be a ‘complete’ verification suite for your FSM in Question 2. Use a different test fixture implementation strategy than the one we have been using so far of relative timing of discrete events. [20 points]