Course Overview & Policies

Off Campus Students
(VBEE and NTU)

Instructor:  Professor Paul D. Franzon, Ph.D.
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Home page :  www.ece.ncsu.edu/erl/faculty/paulf.html

Lab TA/Graders: To be announced.

Textbooks & Notes:
- Course notes, etc. in class locker.
- References:
  - D.J. Smith, `HDL Chip Design", (Doone), ISBN 0-9651934-3-8. (*)

Prerequisite:  Grade of C or better in ECE 212 or equivalent. ECE 406 is useful but not assumed.
Functionally, I am assuming that students are familiar with logic design, including combinational logic gates, sequential logic gates, timing design, Finite State Machines, etc. If you have never designed and verified even a small digital circuit, and remember the principles by which they work, you will be seriously disadvantaged in this class.

Course Objectives. Functionally, the objective of ECE 520 is to prepare you to be an ASIC or FPGA designer in industry. To this end we will focus on how to execute and capture a large complex design in an HDL, using Verilog as the main example. We will also cover a number of other issues important to ASIC designers, including Verification, Design For Test, low power design, etc. You will demonstrate your ability to design a complex ASIC or FPGA function via a major project.
Functionally, the objective of ECE 464 is to give the student advanced preparation in digital system design using HDLs, and introduce other, related, issues. The much simpler project does not fully prepare you to be an industrial designer.

Course Approach:
Lectures: Designed to prepare you for the project and cover issues important to ASIC designers.
Homeworks: The homeworks are designed to either help you gain the skills required for the project or to help prepare you for the exams. Collaboration is encouraged though each student is expected to turn in individual solutions.
Project: A fixed project will be published for each class. The project will be done by the students in pairs. You will be evaluated as a pair.
Written Exams: There will be two multiple choice written exams, a one hour midterm and a three hour final. Both are comprehensive, open-book, open-notes exams.

Compute Resources
You will need access to a Verilog simulator, an appropriate synthesis tool (we use Synopsys), and a suitable ASIC cell or FPGA library. If possible, you should access these resources at your company. If you cannot use this, you can get access to on-campus resources. Please note that without high bandwidth graphical access (or coming to campus), you will find remote access very frustrating. Please contact the VBEE service if you need an on-campus account.

Student Evaluation

<table>
<thead>
<tr>
<th>Item</th>
<th>Postal Date</th>
<th>ECE 520</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homeworks</td>
<td></td>
<td>15%</td>
</tr>
<tr>
<td>Midterm Exam</td>
<td>March, 14</td>
<td>10%</td>
</tr>
<tr>
<td>Project – Prelim Report</td>
<td>April, 4</td>
<td>10%</td>
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<tr>
<td>Project – Final Report</td>
<td>April, 30</td>
<td>30%</td>
</tr>
<tr>
<td>Final Exam</td>
<td>May, 16</td>
<td>35%</td>
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</tbody>
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Each non-exam item can be up to two weeks late with a 10% penalty. After more than two weeks, the item can’t be accepted. I expect the materials to be postmarked by the date above. I will allow one week further for delivery.

Instructor Research Interests
- Interconnect, including transceivers, electronic packaging, on-chip interconnect, optical & electronic interconnect, network switch ICs, MEMS-based interconnect.
- Circuit design, including low-power, SOI, moletronic circuits
- Sample projects:
  - AC Coupled Interconnect
  - On-chip interconnect design
  - Ultra-low power, low-noise SOI radio baseband circuits and architectures
  - Switch architectures for next generation optical networks
  - Molecular circuit design and construction

Students with disabilities
Reasonable accommodations will be made for students with verifiable disabilities. In order to take advantage of available accommodations, students must register with Disability Services for Students at 1900 Student Health Center, Campus Box 7509, 515-7653. [http://www.ncsu.edu/provost/offices/affirm_action/dss/](http://www.ncsu.edu/provost/offices/affirm_action/dss/) For more information on NC State's policy on working with students with disabilities, please see [http://www.ncsu.edu/provost/hat/current/appendix/append_k.html](http://www.ncsu.edu/provost/hat/current/appendix/append_k.html)

Academic integrity
All the provisions of the [code of academic integrity](http://www.ncsu.edu/provost/hat/current/appendix/append_k.html) apply to this course. In addition, it is my understanding and expectation that your signature on any test or assignment means that you neither gave nor received unauthorized aid.