1) Pearl part of HVL not required. (Please do if Pearl working, however)

2) Final post-synthesis verily run will produce SDF errors.
   - Ignore
   - Relax timing (i.e., increase clock period) to get post-synthesis simulation to work.

3) Use edge-triggered flip-flops for all your designs in this class.
latched on falling edge follows on "high" level.
Latch Based Design

Delay from clock going high to φ:

φ-clock φ

Latch (clock edge)

D can not change close to the falling edge.
Set-up and hold times:

D is stored on φ.

Value on D when clock goes low.
D follows D while clock is high.

D-latch
Using the clock-high time like this is called cycle-skewing. If the logic-block connected to Q2 must be proportionally faster then the percentage of time the clock is high is referred to as the duty-cycle.

Notes:

To prevent set-up violations:

Latch timing constraints
Cycle stealing can only be done at a total of half of clock period in a pipeline chain.

- Usually cycle stealing is not allowed and equation on PQ becomes

\[ T_{\text{clock}} > T_{\text{clock}} - \Delta t_{\text{max}} \]

- If cycle stealing is permitted, then the total of all extra delays permitted in a clock of pipeline chains is

\[ T_{\text{clock}} - \text{high-max} \]
Hold violations are harder to prevent in latch-based designs.

Race = Latch Violation.

Note: If

To prevent hold violations:

Latch timing constraints...
1. Determine max clock period.
2. Check for hold violations.

Critical path

Path 1

or

Path 2

Path 1

Q-pin of Flip-Flop.

- Determine max capacitance load. \( C_{ll} \)
- Determine worst case delay

\[
C_l = C_{Q_{max}} + C_{A\phi_{max}} + C_{inv_{max}} \\
(\text{of Flip-flop}) \quad (\text{NOR})
\]

\[
= 11.7 + 37.1 + 20 = 68.8 \text{ fF}
\]

(from Pin Capacitance tables)
Delay of first NIM gate

\[ A \bar{P} \to Y \]

\[ C_{\text{Load}} = 13.6 + 37.1 + 20 = 70.7 \text{fF} \]

\[ t_{\text{logic-max}} = \max(0.598, 0.655) = 0.655 \text{ns} \]

Delay of second NIM gate

\[ C_{\text{Load}} = 52 \text{fF} \]

\[ t_{\text{logic-max}} = 0.615 \text{ns} \]

Path 1

\[ t_{\text{cp-q-max}} + t_{\text{logic-max}} = 1.23 + 0.655 + 0.615 = 2.5 \text{ns} \]

Path 2

\[ Q \to A1 (\text{Not}) \to A\bar{P} (\text{Not}) \to D \]

\[ t_{\text{cp-q-max}} + t_{\text{logic-max}} = 2.58 \text{ns} \]
Worst Case Delay (CP-@)

[Figure 01 or 10]

- Use "delay information tables"

PD = Propagation delay

Note: PD in ns, Cc is in pF

\[
PD = \max \left(1.12 + 1.59 \times Cc, \\
1.09 + 1.52 \times Cc\right)
\]

= \max (1.23, 1.18)

= 1.23 ns.

Cmos circuit

\[\frac{\text{M}}{\frac{1}{C_\alpha} \frac{1}{C_{\text{num}}} \frac{1}{C_{A_o}}}\]
\[ t_{\text{clock-min}} = t_{\text{OPQ-max}} + t_{\text{logic-max}} + t_{\text{tsv-max}} + t_{\text{sleep}} \]
\[ = 2.58 + 1.4 + 1 \]
\[ = 4.98 \mu s \]

\[ \sim 200 \text{MHz} \]

Hold violations

Fastest Path

DFF \( Q \rightarrow \) NOR \( A1 \rightarrow \) DFF \( D \)

D-F1F: \[ C_L = C_{Q\text{-min}} + C_{A1\text{-min}} + C_{\text{wire-min}} \]

D-F1F \( \rightarrow \) NOR

\[ = 5.04 + 15.9 + 10 \]
\[ = 31 \mu F \]
Example:

Assume:

Change: 10 → 20 → F

Ignore details of 0→1 or 1→0 transition
\[ \epsilon_{\text{logic-mm}} = \min \left( 0.18 + 0.258 \times C, 0.162 + 0.451 + C \right) \]
\[ = \min \left( 0.185, 0.171 \right) \]
\[ = 0.171 \text{ ns} \]

\[ \text{Note: Used 21FF} \]

\[ \text{Numbers are wrong.} \]

\[ N \text{or ( } A1 \rightarrow Y) \]
\[ \epsilon_{\text{logic-mm}} = 0.090 \text{ ns.} \]

To prevent hold violations
\[ \epsilon_{\text{hold-max}} + \epsilon_{\text{skew}} \leq \epsilon_{\text{tcp-a-mm}} + \epsilon_{\text{skew-logic-min}} \]

\[ 0.1 + 1 < 0.171 + 0.09 \]
\[ \frac{1.1}{1.1} < \frac{0.26}{0.26} \]
\[ \times \rightarrow \text{HOLD VIOLATION} \]
Fix by inserting extra logic. e.g. chain of inverter.