• VL notes in locker
• No classes next week.

To VBEE/NTU students:

Note: You need to download lecture notes and HWs etc. from class web page.

www.ece.ncsu.edu/courseinfo/ece520-info

[Signature]
The amount of time required to turn $\geq$, into $\leq$, is referred to as timing slack.

Constraint to prevent this:

The right before one set-up time before the clock edge

Logic is too slow for the correct logic value to arrive at the inputs to the register on

Set-up Violation:

Preventing Set-Up Violations
is referred to as "local"
and "hits of Enu" +
Difference between technical
Hold violation illustrated here.

Sometimes have to insert additional logic to prevent hold violations in Q2.

Logic here: we need an extra IF D2 changes before time t_hld.

Clock:

Constraint to prevent hold violations:

Hold violations occur when race-through is possible

Preventing hold violations

ECE 520 Class Notes
Go metastable.

Clock edge delay on output (Q) changing from positive to negative.

Clock edge: Data can not change during this time after point before the clock edge. Data can not change no later than this.

Hold time: 0 becomes D after clock edge.

Setup time: Edge triggered D-flip-flop.

Flip-flop based design.
M.S. Design

Digital Design
ECE 520
ECE 704

Circuit Design
+ ECE 746 +

  ECE 733
  ECE 711
  ECE 79?

  ECE 794

Computer Architecture
+ ECE 521
ECE 743 or 748

Software
CSC 517 - C++
CSC 501 - OS

CSC 550 - Graphics
CSC 510 - SE
Application

ECG 570  Network -576
ECG 713  DSP
714  Random Processes
ECG 747  DSP Architecture

Ph.D.

ECG 738/739 - IC Tech.
ECG 591B  MEMS