assign t = m <= 1

m = 11

→ t 10

0 filled

m m[13]


m[10] t[10]

r: rearranging wires!

//

reg [2:0] u, m;

assign t = {n {m}};

Not Synthesizable

How many copies of m to make? ?

assign t = {4 {m}};
Mux

Incomplete sensitivity list
or "Timing Control" list

Fix: always @ (wor x or y)

All inputs to a block
of CL have to be
in the sensitivity list.
Otherwise, simulation results
might be different
than the actual HW.

always @ (a or b)

begin
    $1 \ c = 1$
    $\text{AND} @$;
    // if (a || b) c = 0;
end

Note:
No latches!
always @ (a or d)
begin
    c = ~a;
    b = c | d;
end

reg [3:0] a;
reg b, c, d;
**Why?**

Each output not being assigned for each combination of I/Ps.

**Fixes**

1. **always @ (w)**
   
   begin
   if2(w)
   \[ z = 1 \text{'}\text{'} b 0; \] // defaults
   \[ y = 1 \text{'}\text{'} b 0; \]
   if \((w)\) \[ z = 1 \text{'}\text{'} b 1; \]
   else \[ y = 1 \text{'}\text{'} b 1; \]
   end

2. **always @ (w)**
   
   if \((w)\) begin \[ z = 1 \text{'}\text{'} b 1; \]
   \[ y = 1 \text{'}\text{'} b 0; \] end
   else begin \[ z = 1 \text{'}\text{'} b 0; \]
   \[ y = 1 \text{'}\text{'} b 1; \] end
reg T1:O3 m,n;
assign q = m | n;

\[ m \rightarrow q \rightarrow n \rightarrow r \]

Logical, Equality
Identity, Relational
- mainly used in
  if else type statements.
assign c = -(a 1 l);