Clock

Count1

mc1 = 1

carry1

next_count1

end

above works OK if mc3 does not change.
Max Delays

\[ \tau_{\text{lenu}} + t_{\text{cp-q}} + t_{\text{su}} + t_{\text{sho}} < t_{\text{clock}} \]

\[ b + 2 + 2 + 1 = 11 \times 10 \]

Setup violation.

\[ \underline{Hold} \]

\[ \tau_{\text{tigc-mm}} + t_{\text{cp-a-mm}} \quad \underline{\leq} \quad \tau_{\text{hold}} + t_{\text{sho}} \]

\[ 1 + 0.5 \neq 1 + 1 \]

Hold violation.
always @(posedge clock)
begin
if (load1) count1 <= in1;
else if (decl & !ended)
    count1 <= next_count1;
if (load2) count2 <= in2;
else if (decl2 & !ended)
    count2 <= next_count2;
end
assign {carry1a, next_count1} = count1 - 1'b1;
assign {carry2a, next_count2} = count2 - in3;
assign ended = (count1 == count2) |
                carry1a |
                carry2a
endmodule
reg [7:0] count1, count2;
wire [7:0] next_count1, next_count2;
wire carry1a, carry2a, ended;