It produced multipliers after optimization, replace newDist = PEcut [PEready << 3+7:
PEready << 3];

Note: Can not pass 2-D array as input - have 1D array.
characterize
determine
  - input delay
  - drive cell
  - output delay
  - output load
for all pins of module specified.
Partioning Example

```vhdl
--current-design = top
--complete
--current-design = ports
characterize constraints [10
group [14 pool] design-name ports-cell-name U10
--current-design = top
--complete
--current-design = top
characterize constraints [10
{ } on worst-case cells/conditions:
//
.....
}(instead of current complete):

Synthesizable Extent:
endmodule:
```

```vhdl
lib mps
module top ()
module top ()
impulse and outputs:
write top level Verilog module (ignoring details of

ECF 520 Class Notes
NC STATE UNIVERSITY
Hierarchy of modules.

Notes:
- bar instance twice as U2 and U3
- circles = combinational logic
- All logic in partition

Partitioning Example
If you do not uniquely all instances of bar will have identical mappings

Why did we uniquely V2

Right # smaller = less multiplied.

Why could you avoid having to do this step at the RTL coding stage?

What could you do to reduce the design size?

Would this strategy lead to the smallest design?

How are the critical path handled?

Based on current design mappings

Determines all constraints (ser-input-delay, etc.) of cell being characterized

Function of characterized?

Comments:

Partitioning Example
What is wrong with this partitioning?